The Valley Megaphone

Newsletter of the
Institute of Electrical and Electronics Engineers, Inc.
Phoenix Section
March 2007, Volume XXI, Number 3

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This Issue of The Valley Megaphone Features:

Contacts:

- **Executive Committee (page 1)**
- **Chapters and Branches (page 1)**
- **Student Branches (page 2)**

Contents:

- **Phoenix Section Executive Committee Meeting (page 2)**
- **AMFA Workshop (pages 3-4)**
- **PDMA Annual Conference (page 5)**
- **Semitracks Courses (page 6)**
- **Student Paper Contest (page 7)**
- **Mentoring Connection (page 8)**
- **RE-SEED (page 9)**
- **WAD Society Meetings (pages 10 - 11)**
- **PACN Meeting (page 12)**

IEEE Phoenix Section Executive Committee meeting minutes can be found at: http://www.ieee.org/phoenix

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.
Advertising Rates: Full page: $200, 3/4page: $125, ½ page: $75, 1/3 page: $50, 1/4 page: $25.
Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

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Embry-Riddle, Prescott
Chair:
Advisor: Chuck Cone
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Phoenix Section Executive Committee Meeting – First Tuesday of the month.

Time: 6:00 pm to 8:30 pm

Place: Phoenix Airport Hilton, 2435 South 47th Street
Phoenix, AZ, 85034
Phone: 480-804-6017

Directions: From 143, exit University Ave, go west, turn right on 47th street.

More Info: Meetings held first Tuesday of month. No meetings in July and August. All interested IEEE members are welcome to attend.

Contact: Rao Thallam, Phoenix Section Chairman, ph: (602) 236-5481 or e-mail: thallam@ieee.org

Advanced Materials/Failure Analysis (AMFA) Workshop

April 20, 2007 • Hyatt Regency Hotel • Phoenix, Arizona

AMFA MISSION:

To serve the interests of failure analysis & materials characterization professionals by providing a forum for the presentation and ***active*** *discussion of timely and pertinent technological issues and trends and to promote the development of new capabilities that fill critical gaps in emerging technologies.*

Unlike traditional conferences that often restrict audience participation, AMFA Workshops provide only top quality invited speakers on leading edge topics, in a format where audience participation is expected and strongly encouraged.

Program

•*Leveraging Federal Funding for Characterization Tools*…….Bruce Gnade, University of Texas, Dallas

This presentation will address funding schemes to develop sophisticated, small volume analytical tools for the semiconductor industry. History has shown us that development cycles of 5-7 yrs and millions of dollars of non-refundable engineering costs are typical. The problem is exacerbated by small world wide sales and the fact that typically the tools are being developed by small, venture capital firms whose budgets are strained. The presentation will include an introduction based on the actual development costs and resources necessary to bring x-ray tomography to the marketplace and the path forward to avoid some of the obvious limitations of that process.

•*"FA Role: Dynamic Driver or Passive Passenger?"*..Rich Blish, Spansion; Efrat Raz, Gemtech

The FA team does not take an active role in technology roadmaps, design reviews, production assessment and post analysis recovery plans and with a limited budget it is expected to continue to support advanced technology and production cost cutting - crying silently in our beer won't change anything! We must demand to become a *technical* partner by developing interactive communication; demanding data and being a follow up partner. The FA manager must be a *business* manager, who markets his/her products aggressively. Success must be communicated both technically and in dollar terms - "top management language".

•*"FA Role: Dynamic Driver or Passive Passenger?"*……..Breakout Discussion

Metrology for Emerging Devices and Materials ……Eric Vogel, University of Texas, Dallas
Scaling of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and its traditional materials has been the basis of the semiconductor industry for nearly 30 years. A wide variety of materials and devices are emerging to extend and replace the traditional MOSFET. This talk will provide an overview of these emerging devices and materials and of the metrology requirements for these technologies

Atomic Level Ion Source Microscopy. . . . . .Bill Ward, ALIS Corp.
A novel helium ion microscope has been developed which has advantages over traditional scanning electron microscopes(SEMs) and focused ion beams (FIBs) for many applications. The ALIS scanning ion microscope uses a beam of helium ions as the imaging particles. Ions can be focused into a smaller probe size - less than 1 nm with a properly designed column, and have less sample interaction than electrons. The ALIS microscope can generate higher resolution images with more material contrast so more detail can be seen. We expect to be able to see things much smaller than we've ever been able to see with even the most sophisticated scanning electron microscope (SEM).

Materials Characterization Using Ultrafast Lasers……...David Cahill, University of Illinois
This presentation describes how the rapid heating of the near surface of metal films by nJ ultrafast optical pulses can be used to generate nanoscale wavelength strain and temperature fields for measurements of the mechanical and thermal properties of thin films and interfaces.

Failure Analysis Year In Review……Christian Boit, Berlin University of Technology
FA innovation trends are measured by IC technology roadmaps. This presentation takes snapshots of the year and introduces major trends. A picture of the dynamics in the different analysis sections metrology, debug/diagnosis on die and package and their respective interactive potential emerges that also anticipates economical aspects of the development.

Registration Fees: $150.00 for IEEE or EDFAS members, $200.00 for non-members. Registration may be done online at www.amfaworkshop.org (after Jan. 01), onsite during IRPS, or at the AMFA Workshop. Registration for the AMFA Workshop includes a CD-ROM of the presented materials, lunch, and morning/afternoon breaks.

The AMFA Workshop is technically co-sponsored by the IEEE Reliability Society and the Electronic Device Failure Analysis Society.

For general workshop information, visit http://www.amfaworkshop.org/ or contact:

Gay Samuelson
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For registration and mailings
IRPS Publishing Services
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Westmoreland, NY 13490 USA
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Fax: (315) 336-9134
e-mail: pub_services@irps.org

pdma

Connecting Innovators Worldwide

March 9, 2007 • 7:30 a.m. to 3:00 p.m. • Edward Jones Training Center • Tempe, Arizona

2007 Arizona PDMA Annual Conference
Innovate Through Sustainable Technologies

Do you truly innovate to make your products green? Do your product development systems take into consideration the design of an eco-effective product and supply chain? Just what does "Sustainability" mean to your company and your products or services? Globalization and sustainability have huge implications in our new "The World is Flat" world. It's not someone else's problem and it's not going away unless we do something about it.

Find out what leading companies such as Dial, Intel, Nature Works, Philips and others are doing to design sustainability into their products.

DIAL
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Premiere Sponsor

Conference Pricing
- $149 Full price
- $25 PDMA/Sponsor membership discount

Become a PDMA Member and receive a special pre-conference panel video

Register at http://www.regonline.com/120154

Edward Jones Training Center
8333 S River Parkway • Tempe, Arizona 85284

Conference Agenda

7:30 - 8:00 am . . . .Breakfast and registration

8:00 - 8:15 am . . . . .Welcome – Dial Corporation

8:15 - 9:00 am . . . . .Govi Rao, VP, Phillips Solid State Lighting

9:00 - 9:45 am . . . . .Doug Kunnemann – Cargill / Natureworks LLC

9:45 - 10:15 am . . . .Networking Break

10:15 - 11:00 am . . .John Potts, Founder Green "T" & CTO, CUSD

11:00 - 11:45 am . . .Wayne Rifer - EPEAT

11:45 - 1:30 pm . . . .Networking Lunch

1:30 - 2:30 pm . . . .John Harland, Intel, "Green Manufacturing"

2:30 - 3:00 pm . . . .Conference Close & Prizes

2007 Annual Conference Sponsors

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Semitracks, Inc. is proud to bring three unique courses to the Phoenix area in April.

Packaging Technology/Challenges
Instructor: Dr. Gay Samuelson
April 9-10, 2007

This course provides an overview of the current business climate, anticipated trends and the associated impact on assembly/packaging.
Topics include the following:

- In depth discussion of several roadmaps and their impact on packaging.
- Assembly flows and cost implications for wafer fabrication and assembly with special focus on low cost alternatives.
- Reliability issues, such as thin film delamination/cracking, bump cracks, via delamination/ cracking, thermal interface degradation, heat sink retention, and socketing issues
- Failure analysis tools, such as SAM, x-ray, SQUID microscopy, TDR, terahertz imaging, thin film materials characterization, and adhesion testing.
- Impact of the latest technologies such as Cu, ultra low k dielectrics, 300mm wafer fabrication, wafer scale packaging, embedded passives, chip on board, and modular integration.
- Future packaging needs for MEMS, and Nanotechnology.

This course is recommended for engineers and scientists involved in the rapidly expanding arena of assembly/packaging in the digital revolution. This course will also be useful to engineers and scientists performing risk assessments on packaging technologies, fault isolation and failure analysis and stress testing to achieve reliability certification of such technologies.

Package Design and Modeling
Instructor: Mr. Steve Groothuis
April 11-13, 2007

This course provides an introduction to assembly/packaging design and modeling process as well as a variety of design and simulation tools used on current technologies.
This class focuses on techniques and the importance of thermal and mechanical simulations. Discussions and examples will concentrate on thermal performance simulations, assembly & packaging stresses, package reliability (including solder joint fatigue simulation), and interactions between chip and package. In addition, a special section will be examples of successful wafer level simulations.
The course covers:

- Current packaging technologies, including chip scale packaging, Ball Grid Array technology and other current concepts.
- Thermal simulations, including modeling power dissipation and thermal diffusivity.
- Mechanical simulations, including thermomechanical interactions and materials thermal coefficient of expansion mismatches.
- Soldering stresses
- Reliability and failure mechanisms
- Package/die interactions
- Wafer level simulations that impact packaging.

This course is recommended for engineers and scientists involved in the design and modeling of packages and package materials, engineers working package/assembly-wafer manufacturing interactions, and reliability engineers.

ESD/Latchup Design & Technology
Instructor: Dr. Steven Voldman
April 12-13, 2007

This course provides an in-depth look at the art and science behind ESD and Latchup Design and Fabrication technology.
Electrostatic Discharge (ESD) and Latchup are a critical concern for the semiconductor and electronics industry. Both ESD and Latchup account for more than $4 Billion in losses each year. This problem is likely to grow in the future as smaller feature sizes are susceptible to damage at lower static voltages and latchup under more subtle conditions.
This course covers:

- Fundamentals and current issues in latchup
- Latchup physics, test structures, characterization, process and technology issues, and new latchup issues in the industry today.
- Fundamentals of ESD. The instructor will first give a background tutorial on ESD physics, electro-thermal and statistical models.
- CMOS, silicon on insulator (SOI) and silicon germanium (SiGe) technologies
- ESD devices, circuits, and process issues in RF CMOS, RF BiCMOS silicon germanium technologies, and gallium arsenide (GaAs).

Participants will also receive copies of Dr. Voldman's books *ESD: Physics and Devices*, and ESD: Circuits and Devices.
This course is recommended for ESD designers, product engineers, reliability engineers, and device technologists.

All three courses will be held at the Hampton Inn and Suites Phoenix/Tempe, 1429 North Scottsdale Road, Tempe AZ, United States, 85281. Tel. 480-675-9799. For more information, or to register for the courses, please visit our website at http://www.semitracks.com/courses/phoenix-courses.htm or call us at 505-858-0454.
Please forward this announcement to colleagues who might be interested.

IEEE Phoenix Section Student Paper Contest 2007

The IEEE Student Prize Paper Contest offers the undergraduate IEEE Student member opportunities to exercise and improve both written and verbal communication skills. Throughout an engineer's career, (s)he will be constantly called upon to communicate ideas to others. Researching, writing, and presenting a paper provides a student with invaluable early experience in expressing ideas related to engineering. Since the paper contest primary function is to improve the engineering student's communicative skills, no student should be discouraged from entering the contest due to a false requirement of technical sophistication.

This undergraduate student paper contest consists of a written paper and an oral presentation. The written paper should be in the IEEE region 6 standard, which is available at http://www.ewh.ieee.org/reg/6/MemberStudentActivities/IEEERegionalStudentPaperContestGuidelines.doc . Briefly, the type-written papers are 15 pages maximum, double-spaced with 12 pt font. The written paper, as either an MS Word or an Acrobat pdf file, should be emailed to jdrye@ieee.org by 6 p.m. on **March 3, 2007**.

The oral presentations are 15 minutes plus a 5-minute question & answer period. The oral portion of the contest to be held the morning of Saturday **March 17, 2007**, at the ASU Tempe campus in the ASU Memorial starting at 8 a.m. A computer with projector will be provided for the contestants to use, since PowerPoint slides are the recommended approach. The best place to park that day should be the visitor section of Parking Structure 1 which is located near the intersection of Apache Blvd. and Normal St., and which is a short walk to the south of the Memorial Union (see http://www.asu.edu/map/).

The local cash awards for the paper contest winners are (1) First Place – $300, (2) Second Place – $200, and (3) Third Place – $100. The five judges are IEEE members from local industries.

The top entrant from each Local Student Branch (ASU Main, ASU Polytechnic, DeVry, Embry-Riddle, and NAU) is eligible to present their paper to the IEEE Region 6 Southwest Area contest to be held April___ in Las Vegas, NV.

If you have any questions, please contact:

Jim Drye
Student Activities Chair
Phoenix Section

Voice: (480) 413-5685
Email: jdrye@ieee.org

IEEE Mentoring Connection

IEEE is offering its members the opportunity to participate in an online program which will facilitate the matching of IEEE members for the purpose of establishing a mentoring partnership. By volunteering as a mentor, individuals use their career and life experiences to help other IEEE members in their professional development. I believe this program can be a great tool to provide our newest members of our profession guidance in their careers and provide experienced members a chance to hear first hand from the newly graduated about the latest training the next generation is receiving. This is a program for higher level members and is provided to help ease the transition out of school and into a career.

As a mentee, you lead your partnership by selecting your mentoring partner from among those who have volunteered to serve in this capacity. I ask that you review the time and effort commitment to the program to ensure a successful mentoring partnership. Participation in the program is voluntary and open to all IEEE members above the grade of Student Member.

If you are interested, please go to http://www.ieee.org/mentoring for information on the roles and responsibilities of each mentoring partner. I encourage you to take advantage of the IEEE network of technical professionals or offer your expertise and sign up for the online mentoring program today.

Who can be an IEEE Mentor?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Able to communicate effectively with others
- Willing to share some career successes and failures
- Individuals who may be or have been executives, consultants, or in middle or upper management, or in research
- Individuals who may be or have been educators, entrepreneurs, or self-employed
- Individuals who may be or have been proven leaders offering inspiration and insight
- Individuals who may be or have been IEEE officers or volunteers
- Willing to review an orientation session to learn guidelines, tools of program and the mentee and mentor's role and responsibilities

Who can be an IEEE Mentee?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- New professionals in their first or second job, or considering entering graduate programs
- Recent graduates entering the professional workforce for the first time
- Professional making a career move or career change
- Passionate for learning
- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Willing to identify and clarify their developmental goals
- Interested in learning from another professional "who has been there"
- Willing to participate in mentee orientation session to learn guidelines, and tools of program and their role and responsibilities as a mentee

This program deserves your consideration and doesn't require a large amount of time on your part. It can provide of great assistance to the next generation of engineers.

Russ Kinner
Membership Chair, Phoenix Section

Volunteer Opportunity for Retired Members

There is a volunteer opportunity for retired members of the IEEE in the valley. RE-SEED (Retirees Enhancing Science Education through Experiments and Demonstrations) is seeking volunteers. The organization will be conducting training for volunteers at the Chandler Unified Schools in conjunction with Arizona State University. The all day workshops will take place Monday, March 19-Thursday March 22, 2007. They are hoping to have 15-20 engineers or scientists take part in it and they will then be placed in Chandler schools as volunteers. If interested, please contact Shelia Kirsch at Sheila.Kirsch@asu.edu and / or Deirdre Weedon, d.weedon@neu.edu. See also the web site: www.reseed.neu.edu or phone: 1-888-742-2424

RE-SEED

Retirees Enhancing Science Education through Experiments & Demonstrations

Overview

RE-SEED (Retirees Enhancing Science Education through Experiments and Demonstrations) is a Northeastern University program that prepares engineers, scientists, and other individuals with science backgrounds to work as volunteers, providing in-classroom support to upper elementary and middle school science teachers with teaching the physical sciences.

After completing a comprehensive free training program, participants volunteer in middle school classrooms on the average once a week for at least one year. RE-SEED began in 1991 with six volunteers. To date close to 500 RE-SEED volunteers have worked in schools in about 100 communities throughout the country offering about 500,000 hours of their time.

Nationally, 75 percent of 7th and 8th grade students are taught physical science by teachers who do not have a major or a minor in the subject (The National Science Board, Science and Engineering Indicators 2000). RE-SEED volunteers possess talent and expertise that complement those of science teachers. They bring with them a wealth of knowledge and experience that allows them to make science interesting and relevant to everyday situations.

RE-SEED volunteers work closely with the host science teachers to help them enrich and implement their school curriculum. Overall the volunteers become involved members of their schools' and even their districts' teaching team, sometimes taking part in curriculum adoption decisions.

Please contact us by email at reseed@neu.edu or phone 888-742-2424; Shelia Kirsch at Sheila.Kirsch@asu.edu and / or Deirdre Weedon, d.weedon@neu.edu. if you are interested in learning more about these training programs.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

WAVES AND DEVICES
PHOENIX CHAPTER

March 8, 2007 MTTS Meeting

www.eas.asu.edu/~wadweb

RF CMOS Research at the University of Michigan

Michael Flynn
Wireless Integrated Microsystems NSF Engineering Research Center

Abstract

The presentation will deal with two papers presented by the group at ISSCC - a self calibrated, fully integrated 2.4GHz CMOS super-regenerative receiver, and a digital dominant Frac-N PLL modulator

A 2.2GHz fractional-N synthesizer with a digital phase detector and a dual switching scheme is presented. An additional feedback loop incorporating phase oversampling helps to achieve a measured noise performance of -133dBc (-106dBc) at a 10MHz (1MHz) offset. The MSK modulation rate is 927.5kb/s. The 0.7mm2 prototype IC, implemented in a 0.13µm CMOS process, consumes 14mW from a 1.4V supply.

Super-regeneration is re-examined for its simplicity and power efficiency for low-power, short-range communication. A fully-integrated super-regenerative receiver in 0.13 /µ/m CMOS is designed to operate in the 2.4 GHz ISM band. A frequency synthesizer scheme tunes the pass band. Successive approximation register (SAR) logic driving a current Digital-to-Analog Converter (DAC) calibrates the quench signal to enhance the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. A single-chip prototype receiver occupies less than 1 mm^2 , has a turn-on time of 83.6 /µ/s, a channel spacing of 10 MHz, and a sensitivity of –90 dBm. A data rate of 500 kbps is achieved with a power consumption of 2.8 mW, corresponding to energy consumption of 5.6 nJ per received bit.

Biography

Michael P. Flynn was born in Cork, Ireland. He received the B. E. and M. Eng. Sc degrees from the National University of Ireland at Cork, in 1988 and 1990 respectively. He received his Ph.D. degree from Carnegie Mellon University in 1995.

From 1998 to 1991, he was with the National Microelectronics Research Centre, Cork. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995. From 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, DSP R&D lab, Dallas, TX. During the four year period from 1997 to 2001, he was with Parthus Technologies, Cork, where he held the positions of Technical Director and Fellow. During that time, he was also a part-time faculty member at the Department of Microelectronics, National University of Ireland (UCC), Cork. Dr. Flynn joined the University of Michigan in 2001. His technical interests are in data conversion, gigabit serial transceivers, and RF circuits.

Dr. Flynn received the 1992-93 IEEE Solid-State Circuits Pre-doctoral Fellowship. He received the NSF Early Career Award in 2004. In March 2006, he received the 2005-2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He was Associate Editor of the IEEE Transactions on Circuits and Systems II from 2002 to 2004. He is an Associate Editor of the IEEE Journal of Solid State Circuits (JSSC) and serves on the Technical Program Committees of the International Solid State Circuits Conference (ISSCC) and the Asia Solid State Circuits Conference (A-SSCC). He is a Senior Member of the IEEE, a member of Sigma Xi. He is Thrust Leader responsible for Wireless Interfaces at Michigan's Wireless Integrated Microsystems NSF Engineering Research Center.

Date: Tuesday March 8, 2007
Location: Bernoulli Conference Rm, Bldg 99, Freescale Semiconductor, 2100 E. Elliot Rd., Tempe
Drive North on Country Club off Elliot on the western edge of the Freescale site, enter back parking lot
Time: 3:30 - 4:30pm Presentation
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

IEEE

WAVES AND DEVICES
PHOENIX CHAPTER

March 9, 2007 MTT-S Meeting

Piezoelectric Contour-Mode Vibrating RF MEMS

Gianluca Piazza
University of Pennsylvania
piazza@seas.upenn.edu

Abstract

Recent advancements in the field of wireless communications have dictated the need for new micromechanical RF components capable of multi frequency low loss filtering and frequency synthesis. The growing demand for newer functionalities and applications has crowded the frequency spectrum to the point that several RF bands are now closely spaced within a few MHz. These needs translate in performance requirements in terms of insertion losses, rejection, integration, and quality factor that state of the art resonator technologies such as SAW and FBAR can hardly meet altogether. A new class of aluminum nitride vibrating RF MEMS resonators has emerged as a potential solution for next generation wireless communications. These devices have their fundamental frequency set by their in-plane dimensions and therefore dubbed contour-mode resonators. AlN contour-mode resonators are the only MEMS structures capable of spanning frequency from 10 MHz up to GHz (in their fundamental mode of operation) on the same silicon chip and demonstrating impedance values on par with existing technologies and therefore readily matched to 50 Ω RF systems.

This talk will cover the basics of piezoelectric contour-more resonators and filter design and present initial experimental results using these devices for circuit applications such as band pass filtering and frequency synthesis. Furthermore, new architectures for RF front-ends characterized by reduced power consumption and faster switching speed levels that are enabled by these devices will be introduced. The ability to batch fabricate filter banks at different frequencies will deliver compact and highly integrated solutions capable of frequency hopping and direct frequency synthesis in next generation reconfigurable radios.

Biography

Gianluca Piazza is an Assistant Professor in the department of Electrical and Systems Engineering (ESE) at the University of Pennsylvania. His research interests focus on piezoelectric micro and nano systems (MEMS/NEMS) for RF Wireless Communications, Biological Detection, and Wireless Sensor Platforms. He also has general interest in the areas of micro/nano fabrication techniques and integration of micro/nano devices with state-of-the-art electronics. He received his Ph.D. degree from the University of California, Berkeley in 2005, where he developed a new class of AlN contour-mode vibrating microstructures for RF communications. He has more than 7 years of experience working with piezoelectric materials. He holds two patents in the field of micromechanical resonators and has recently co-founded a start-up (Harmonic Devices, Inc.) aiming at the commercialization of single-chip and multi-band RF filters and oscillators.

Date: **March 9, 2007**
Location: **Group Conference Rm, Bldg 94, Freescale Semiconductor, 2100 E. Elliot Rd., Tempe, AZ**
Use Freescale Main Entrance on Elliot Road
Time: **3:30 – 4:30 pm Presentation**
For more information, please call Sergio Pacheco (Chapter Treasurer) at (480) 413-3737.

IEEE Phoenix Area Consultants Network March Meeting: Flexible Displays – New Developments in Technology

Date: Thursday, March 8th, 2007

Time: Networking begins at 6:30 pm
Dinner begins at 7:00 pm
Program starts at 8:00 pm

Place: Monti's Restaurant
1 Rio Salado Parkway
Tempe, Arizona

Abstract: Edward J. Bawolek, Principal Test Engineer at the Flexible Display Center at Arizona State University will present: "Active Matrix TFT Technology Development and Pilot Line Manufacturing for Flexible Displays." This is a reprise of a talk originally presented by Dr. Greg Raupp (FDC Director) at the USDC Flexible Displays and Microelectronics Conference Phoenix, Arizona, February 6-8, 2007.

Please RSVP by noon on Monday the 5th to Vaughn Treude, vaughn@nakota-software.com. For more information about the Consultants Network, see the IEEE PACN website, ieeepacn.com.