The Valley Megaphone

Newsletter of the
Institute of Electrical and Electronics Engineers, Inc.
Phoenix Section
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This Issue of The Valley Megaphone Features:

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Contents:

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.
Advertising Rates: Full page: $200, 3/4page: $125, ½ page: $75, 1/3 page: $50, 1/4 page: $25.
Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

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Embry-Riddle Computer Society
Advisor:

ECTC 2006

The 56th Electronic Components and Technology Conference

May 30 - June 2, 2006
Sheraton San Diego Hotel & Marina
San Diego, California USA

Introduction

It is my pleasure to invite you to submit an abstract for the 56th Electronic Components and Technology Conference (ECTC), to be held May 30 - June 2, 2006 in San Diego, California. This premier international conference is sponsored jointly by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and the Electronic Components, Assemblies, and Materials Association (ECA), the electronic components sector of the Electronic Industries Alliance (EIA). You are not required to be a member of either organization to present a paper or attend the conference.

The ECTC comprises papers covering a wide spectrum of topics, including electronic components, materials, assembly, packaging, system packaging, optoelectronics, reliability, and simulation. We have also included a topic on emerging technologies in the program to address exciting new developments and applications. A plenary session and a panel discussion address selected topics each year. Authors from companies, research institutes, and universities located around the world presented more than 300 papers and posters at the 2005 ECTC to about 1,000 conference participants.

Professional Development Courses covering 16 different topics are offered by world-class experts in their fields. Participants can catch up with new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the technical exhibition corner. Leading companies primarily in the electronics components, materials, and packaging field exhibit their latest technologies and products.

The ECTC Program Committee represents a wide range of disciplines and expertise from the electronics industry. I would like to encourage you to submit an abstract on your recent, previously unpublished work to the 56th ECTC at www.ectc.net. The deadline for abstract submission is October 15, 2005. I look forward to seeing you in sunny San Diego, California in May 2006.

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For information about past proceedings (printed or CD-ROM), visit the ECTC website www.ectc.net.

Visit the ECTC website (www.ectc.net) for additional conference information.

Major Topics

Papers presenting new developments and knowledge in the following areas are invited. Please select two subcommittees that should consider your paper. *The work submitted should be original and not previously published, and avoid the inclusion of commercial content.*

- *Advanced Packaging:* New packaging technologies, systems packaging, first level thermal solutions for high power applications, designs, materials, and configurations addressing performance, density and cooling for single chip, multichip, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pb-based and Pb-free bumps and package assembly.
- *Components & RF:* New passive or active component technologies, integrated-embedded components, RF and wireless component applications, modules with subsystem functionality, component performance, and reliability.
- *Education:* Education for engineering curricula in the 21st century and collaborative research and engineering programs between universities, government, or industry; development and the use of multimedia for packaging education.
- *Emerging Technologies: Biomedical, Nano-Scale and Organic Device Packaging:* Packaging of biomedical and bio-sensing devices, micro-fluidic devices, bio-compatible materials, micro-to-nano transition, nano-electro-mechanical systems (NEMS), organic electronic devices (active and passive), and systems. Materials, fabrication, characterization, optical properties, packaging, and reliability. Applications nano fluidics, optics, and mechanics, RFID, electronic papers, flex circuits, bio-compatibility. See next page for more information.
- *Interconnections:* First-level electronic interconnection technologies including flip-chip, lead-free, fine pitch bump, wafer level and novel interconnection structures and processes, MEMS interconnect, under bump metallurgy, high density (HDI) substrate interconnect, wirebonding, conductive polymers for interconnect, interconnections for 3D stacking (SIP/SOP), interconnection for new Silicon technologies (e.g. low-k), thermal, mechanical, and electrical aspects of interconnect structures, electromigration of bumped interconnects.
- *Manufacturing Technology:* Advanced process development and equipment improvement for wafer thinning, bumping, stacking; low-k chip and sensor packaging; high-density interconnect and embedded component substrates; testing and burn-in. Emphasis on product level integration and optimization for different product applications, cost, yield, performance and environmental improvements, process characterization, new product introduction and ramp, design for flexible manufacturing and testing.
- *Materials & Processing:* Processes for IC Packaging that enhance performance (mechanical, thermal and electrical) and cost effectiveness. These include new technologies, development and application of adhesives, encapsulants, chip underfills, solders and alloys, magnetic and optical materials, thermal interface materials, ceramics, composites, dielectrics, thin films, nanomaterials to bonding, plating and other assembly processes.
- *Modeling & Simulation:* Electrical, thermal, optical, mechanical modeling, simulation, characterization and packaging solutions including system-level applications.
- *Optoelectronics:* Packaging for fiber-optic modules, optical devices and components including optical amplifiers, lasers, detectors, OEICs, and passive components, non-hermetic and plastic optical packages, optoelectronic package manufacturing, materials, fabrication and process technology, solid state lighting (LEDs and display arrays), optical data interconnects, WDMs, fiber-to-the-home, arrays and broad area lasers and optical back-planes.
- *Posters:* Papers may be submitted on any of the listed major topics; presentation of papers in a poster format is highly encouraged at ECTC.
- *Quality & Reliability:* Reliability assessment and prediction at the system, PWB or package level; reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; interconnect reliability physics, testing and predictive simulation; advances in reliability test methods and failure analysis.

Professional Development Courses

Proposals are also solicited from individuals interested in teaching educational short courses (4 hours) on topics described in the Call for Papers.

Proposals including course descriptions must be submitted by October 15, 2005 via the website at www.ectc.net. For more information please contact Ricky Lee, phone +852-2358-7203, rickylee@ust.hk.

Paper Submission

You are invited to submit a 750 word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. Please check the website for details on how to submit abstracts electronically. For additional information regarding abstract and paper submissions, please contact torsten@astri.org.

The abstracts must be received by **October 15, 2005.** Your submission must include the mailing address, business telephone number and facsimile number, and email address of the presenting author and affiliations of all authors. Please indicate no more than two program subcommittees that should evaluate your paper for acceptance. Authors will be notified of paper acceptance with instructions for publication by December 19, 2005. At the discretion of the program committee, abstracts submitted may be considered for poster sessions.

Manuscripts are due in final form for publication in the Conference Proceedings by February 3, 2006. **The work submitted should be original and not previously published, and avoid inclusion of commercial content.** In addition to a printed copy conforming to the ECTC format, a computer file for the CD-ROM is needed in the preferred MS Word format.

Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose author(s) receive an ECTC personalized wall plaque and share a check for $2500.

Best Poster Award: Each year the ECTC selects the best poster paper whose author(s) receive an ECTC personalized wall plaque and share a check for $1500.

Outstanding Paper Awards: Other outstanding conference papers are also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1000.

Outstanding Poster Awards: Other outstanding poster papers are also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1000.

Intel Best Student Paper Award: Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at the ECTC. The winning student will be presented with a wall plaque and a check for $2500.

IEEE CPMT Transactions: In addition to the publication of papers in the Conference Proceedings, a selection of the top papers is published in a special issue of the IEEE CPMT Transactions.

Technology Corner Exhibits

Reserve Your Space Early!

Exhibit your products or services to more than 1,000 engineers and managers from all electronic disciplines including: Packaging, Interconnections, MCMs, Hybrids, Thermal Management, Modeling, Quality, Reliability, Materials, Processing, Components and Optoelectronics. One and one-half days, May 31 & June 1, 2006. More than 70 percent of the 68 booths available have been reserved by 2005 exhibitors. For information and an application, contact Bill Moody by email: b.o.moody@ieee.org

Advance Programs will be available February 2006.
Contact Steve Bezuk, Kyocera America Corporation,
8611 Balboa Ave., San Diego, CA 92064.
Phone (858) 576-2651, Fax: (858) 569-9412,
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Emerging Technologies: Biomedical, Nano-Scale Packaging and Organic Device Packaging

As part of the ECTC Program Committee's commitment to provide coverage of advanced and emerging technologies, we are soliciting abstracts for the 2006 ECTC on three special topics: "Biomedical Packaging," "Nano-Scale Packaging" and "Organic Device Packaging." When you submit your abstracts on the ECTC website, www.ectc.net, select "Emerging Technologies" as the primary review committee.

Biomedical packaging is experiencing increased interest as the devices are shrinking and more point-of-care biochips are being developed with integrated capabilities for diagnostics, drug delivery, precision surgery, prosthesis, as well as pathogen and bio-sensing. Platforms that integrate biological processing, transducers, circuits, and communications require special packaging that can handle microfluidic as well as microelectronic and optical systems. The conference is especially interested in presentations describing integration of functionality as well as miniaturization of the devices. Abstracts are being solicited for development of packaging for these devices that cover device design, materials, fabrication methods, and complete packaging of biomedical and other biotechnology systems, especially in regards to miniaturization, integration, biocompatibility, disposable applications, measurement and testing.

Nano-scale technologies are being developed for the next generation of devices. Packaging and interconnect of these nano-scale devices need to be developed, including the nano-to-micro transitions and interfaces. At the same time, nano-scale structures are being developed and are enabling new interconnect methodologies. Abstracts are being solicited for both packaging of nano-devices, such as high-sensitivity gas and biosensors, as well as development of the new generation of materials for interconnect and packaging materials that utilize nanosize structures such as carbon nanotubes and nanowires. The topic is calling for devices, materials, and processes that result in or support submicron size structures. Some specific topics of interest include use of nanowires for interconnect, nanopatterning technologies, NEMS, nanofluidics, and special properties at nano-scale such as nanomagnetism.

Organic device technology is developing rapidly, especially for low-cost applications. Similarly, organic LEDs and optoelectronic systems show great promise. Polymers have long been key packaging materials, and organic electronics offer the opportunity to embed active devices with passives, and to merge device and packaging technologies. Papers are sought in all areas of organic device technologies.

14th Motorola-IEEE CPMT Society Graduate Student Fellowship for Research on Electronic Packaging

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) is pleased to announce a Fellowship for Research on Electronic Packaging sponsored by Motorola, Incorporated.

Description: The purpose of the Fellowship is to promote graduate-level study and research on electronic packaging. An annual award will be made to a student enrolled full-time in a graduate curriculum leading to a Ph.D. and whose major field of interest is in electronic packaging. For the purpose of this award, electronic packaging research is defined as the fundamental study of the design analysis or characterization, construction, manufacturing, or reliability of the electronic interconnection of semiconductor or photonic devices, or the thermal management of mechanical assembly of said devices. All forms of electronic packaging are included, from low power to high power, low performance to high performance, including applications ranging from computers, telecommunications, and aerospace to automobiles and manufacturing systems as they relate to electronic packaging.

Eligibility: Candidates must have completed a minimum of four years of college (U.S. and/or non-U.S. colleges, universities or institutes) and a year of graduate study in a recognized engineering or scientific curriculum. They must be enrolled in a doctoral program whose major field of interest is in electronic packaging.

The award will be based on a student paper competition to be conducted in the Electronic Components and Technology Conference (ECTC) which is sponsored jointly by the CPMT Society of the IEEE, and the ECA. Students must submit abstracts to the Program Committee of the ECTC in accordance with the ECTC "Call for Papers" and indicate desire to be considered for the Motorola Fellowship on their abstract.

Travel Support: The IEEE CPMT Society will provide travel reimbursement of up to $1000 for seven Fellowship finalists, chosen based on submitted manuscripts. Fellowship candidates not chosen as finalists may be provided up to $500 in travel reimbursement. ECTC conference registration fees will be waived for all seven Fellowship finalists.

For information regarding the Fellowship, please contact Andrew Skipor at aas002@email.mot.com.

Nominations Solicited for IEEE CPMT Society Awards

CPMT Society solicits nominations for the following awards for the year 2006. These awards are offered for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society. For nomination guidelines, basis of judging, and further information about the awards, please visit the website http://www.cpmt.org/awards. Nomination forms can be obtained from the website, or from the CPMT awards committee chair. Minimum **three** reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members. **The due date for receiving the nominations is January 31, 2006.**

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
Prize: $2,500 and Certificate
Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2005.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2005.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Eligibility: No need to be a member of IEEE and CPMT Society.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
Prize: $2,500 and a Certificate.
Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2005. There are no requirements for service to the IEEE or CPMT Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2005, and must be 35 years of age, or younger, on December 31st, 2005.

Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

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Email address: r.bonda@ieee.org or rao.bonda@freescale.com

Winners will be notified by February 28, 2006 and the awards will be presented at the 56th Electronic Components and Technology Conference, May 30- June 2, 2006, in San Diego, California, USA.

January Meeting Announcement for the Phoenix Chapter of the IEEE EMC Society

Date: Wednesday, January 25th
Place: Embassy Suites Hotel
Address: 4400 South Rural Road, Tempe, Arizona
Address: Just South of U.S. 60 on West side of Rural Rd.
Time: 1:00PM - 7:00PM (12:45PM Registration)
Title: Tech Tour: Aerospace EMC**,** A Half-Day Technical Seminar with Demonstrations

The Phoenix Chapter of the IEEE EMC Society is pleased to host this event with leading industry experts including James Young of Rohde & Schwarz, Vince Rodriguez of ETS-Lindgren, and Harry Gaul of General Dynamics C4 Systems.

Program Outline

12:45 Registration

1:00 The Influence of Ground Plane Reflection on Antenna Calibration and Measurements by Harry Gaul, General Dynamics C4 Systems

This presentation will provide the theory and details of performing antenna calibrations in both free space and ground plane configurations in accordance with standards such as ANSI C63.5 and SAE ARP958. The concept of Normalized Site Attenuation (NSA) will be introduced as a means to derive the difference between free space and ground plane test configurations. Antenna range measurements will also be discussed from the standpoint of how to include the effects of reflection from earth with finite conductivity.

2:30 Break

2:45 Anechoic Chamber Solutions for Antenna Pattern Measurements by Vince Rodriguez, ETS-Lindgren

This presentation introduces the user to antenna ranges, and concentrates on rectangular and taper anechoic chambers for APM. Absorber technology, Quiet Zone levels, and far field requirements are discussed as well as the proper absorber treatment for both taper and rectangular chambers.

4:00 Break

4:15 Improving the Accuracy of EMI Measurements by James Young, Rohde & Schwarz

Topics to be addressed include: "The Spectrum Analyzer versus The EMI Receiver" (advantages and disadvantages), plus, the problems and benefits of using low noise amplifiers for increased sensitivity will be reviewed.

5:30-7:00 RECEPTION WITH THE SPEAKERS, HANDS ON DEMOS OF THE MATERIAL PRESENTED, RAFFLE FOR PRIZES!

About the Speakers:

Harry W. Gaul, P.E., is the EMC/TEMPEST Group Technical Manager for General Dynamics C4 Systems in Scottsdale, Arizona. He is a Registered Professional Engineer (PE) in the state of Arizona and is a NARTE Certified EMC Engineer. He is also the IEEE EMC Society Chapter Chair for the greater Phoenix area. Mr. Gaul has been involved in EMC, EMP, ESD and TEMPEST test and design engineering for more than 20 years. He received the B.S.M.E. degree from the University of Colorado in 1978 and the Technology M.B.A. degree from Arizona State University in 1998.

Vicente Rodríguez-Pereyra of ETS-Lindgren was born in Madrid, Spain. He obtained his BSEE from the University of Mississippi in 1994. He joined the department of EE at the University of Mississippi as a research assistant. He was involved in projects addressing the reduction of cross talk in high-speed digital circuits and the use of the Finite Difference Time Domain technique in antenna analysis. During this time he obtained the MS and Ph.D degrees in Engineering Science with an emphasis on Electromagnetic Theory in 1996 and 1999, respectively. In August 1999, Dr. Rodriguez joined the department of Electrical Engineering and Computer Science at Texas A&M University-Kingsville as a Visiting Assistant Professor. In June 2000, Dr. Rodriguez left the academic world and joined EMC Test Systems (now ETS-Lindgren) as an RF and Electromagnetics engineer. He is the author of more than 20 technical publications. Dr. Rodriguez is a member of the IEEE and several of its technical Societies including the MTT and the EMC Societies. He is also an active member of the Applied Computational Electromagnetic Society (ACES). Dr. Rodriguez is a full member of the Sigma Xi Scientific Research Society and of the Eta Kappa Nu Honor Society.

James Young is the sales and marketing manager for Rohde & Schwarz EMI products in the Americas. His engineering background includes system, circuit, ASIC and FPGA design for various communication products. He has also held product management and marketing positions with Cadence (Tality) in San Jose, CA, ParkerVision in Jacksonville FL, and Signal Space Design in Salt Lake City, UT. He holds a BSEET from Weber State University and an MBA from the University of Phoenix.

The Program Format:

The half-day will consist of a three part technical seminar. The goal of the seminar presentations is to provide practical information for the EMC engineer, designer or technician to actually use on the job! Following the technical seminar, a reception with the speakers will be held in a neighboring section of the hotel. Demonstrations of the material presented will be conducted. Participants can informally meet with the speakers and view these hands on demonstrations that are designed to "drive home" the material presented. Heavy appetizers will be served and two drink tickets per person will be provided for the open bar. (After that, the bar converts to a "cash bar" basis.) A door prize drawing will be held at the conclusion of the reception. Drop your business card in the bowl on the registration desk and enter to win the door prize. You must be present to win, of course!

There is no charge to attend this seminar, but a completed registration form must be on file in order to be admitted to the seminar. Seating is limited; seating will be reserved on a first come, first served basis. *NOTE: The speakers and program may be subject to change without prior notice.*

REGISTER ON LINE at www.techtoursite.com

Please visit our web site at http://www.ewh.ieee.org/r6/phoenix/phoenixemc/index.html for more information.

S A I N T 2 0 0 6 Call For Participation

The 2006 International Symposium on Applications and the Internet

January 23-27, 2006

Mesa, Arizona, USA

Co-sponsored by the IEEE Computer Society (IEEE-CS) and the
Information Processing Society of Japan (IPSJ)

http://www.saintconference.org/ and http://infonet.cse.kyutech.ac.jp/conf/saint06/

The SAINT2006 Organizing Committee welcomes you all to Mesa, Arizona with 41 symposium paper presentations selected from 99 submitted papers, keynote speeches, 5 workshops on cutting-edge topics, 3 panel discussions, covering a diverse range of applications and their enabling Internet technologies.

Make your registration and hotel reservation as soon as possible

For your Registration and Hotel Reservation:
From SAINT Generic Page: http://www.saintconference.org/
> SAINT2006 Homepage > Go to Registration Page
Or
http://infonet.cse.kyutech.ac.jp/conf/saint06/registration/index.html

THEME: Pervasiveness and Diversity of the Internet

Over the past few years, the Internet has been revolutionizing the way we communicate by technical advances such as fiber optic networks, high- speed IP switching, DSL and CATV broadband accesses, along with the increasing performance of PCs, mobile terminals, etc. This growth has helped to identify the need for the Internet to support a diverse range of communications and to accommodates a wide variety of information, services, people, communities, and cultures. The Internet is also becoming to be ubiquitous and pervasive; accessible and usable from any device and through any network, including wireless and mobile. SAINT focuses on emerging and future Internet applications and their enabling technologies.
The symposium provides a forum for researchers and practitioners from the academic, industrial, public and governmental sectors, to share their latest innovations on Internet technologies and applications. Areas of particular interest include:

- Internet Agents
- Collaboration Technology
- Internet Content Management Systems
- Content Delivery
- E-business
- Wireless and Mobile Internet
- Standards for Internet Applications
- GRID Computing
- Internet Appliances
- Novel Internet Applications
- Internet Security
- Network and Protocol Architecture
- Internet Operation and Performance
- Universal Accessibility
- Other Internet Services

Keynotes:

(to be informed on the web soon)

Workshops:

SAINT2006 will feature workshops to provide forums for researchers and practitioners to share knowledge and exchange ideas on cutting-edge topics in Internet and applications. Papers selected by SAINT workshops will be published in a separate volume as an integral part of the SAINT2006 proceedings. There is only one registration fee for both the main conference and workshop participants who can attend any conference sessions.

The following 5 workshops are anticipated:

1: IPv6 Deployment of Technologies and Applications
2: Network Security Threats and Countermeasures
3: Next Generation Service Platforms for Future Mobile Systems (SPMS 2006)
4: Ubiquitous networking and enablers to context aware services
5: RFID and Extended Network; Deployment of Technologies and Applications

Panels:

(to be informed on the web soon)

Organizing Committee:

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Shinji Shimojo, Osaka Univ., Japan
Joseph Urban, Arizona State Univ., USA
Program Chairs:
Patrick Bobbie, Southern Poly St Univ, USA
Haruo Takemura, Osaka Univ., Japan
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James Kempf, DoCoMo Comm. Labs., USA
Steering Committee Chair:
Yuji Oie, Kyushu Institute of Tech., Japan

IEEE PHOENIX SECTION
ANNUAL BANQUET
Saturday, February 11th, 2006
At

Hilton Phoenix Airport
Grand Ballroom
2435 South 47th Street
Phoenix, Arizona 85034
Tel: (480) 894-1600

Program:	6:00 PM – 7:00 PM	Registration and Social Hour with Cash Bar
	7:00 PM – 8:30 PM	Dinner and Keynote Presentation
	8:30 PM – 9:30 PM	Awards Program

Keynote Speaker: Prof. Neville Woolf
Professor, Department of Astronomy, Steward Observatory
University of Arizona, Tucson, Arizona

Keynote Presentation: Telescopes of the Future: Expanding the Frontiers of Astronomy

AWARD RECOGNITION CATEGORIES

Member
Young Engineer of the Year
Engineer of the Year

Advance Member Grade
Fellows, Senior Members

Chapter/Society
Individuals, Teams, Organizations, Best Society Chapter

Non-IEEE Member
Contributions to the Engineering Profession

Corporate
Large Company of the Year
Small Company of the Year

Education
Outstanding IEEE Student Branch
Outstanding Faculty
Outstanding Pre-College Educator
Phoenix Section Student Scholarships

Special Chair
Chair Special Recognition
Phoenix Section 2005 Officers

Future Cities Competition
Phoenix Section Communication Award

Banquet Fees:

IEEE Members and Guests	$30.00	IEEE Student Members	$20.00
IEEE Student Member Guests	$30.00	IEEE Chapter / Society Table	$240.00*
Corporate Sponsorship	$500.00**		

*Table sits 8 persons
**Sponsorship includes recognition at program, table of eight for dinner, and space for display
The deadline for receiving the registration fee is **Friday, February 3rd, 2006**

For Making Reservations and Sending Checks Please Contact:
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437 East Tonto Place
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For Further Information Please Contact Annual Banquet Organizing Committee Members:

Dr. Vasudeva P. Atluri	(480) 554-0360
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For more information visit our web page: http://www.ieee.org/phoenix

IEEE PHOENIX SECTION
ANNUAL BANQUET

Saturday, February 11th, 2006

At

Hilton Phoenix Airport
Grand Ballroom

2435 South 47th Street
Phoenix, Arizona 85034
Tel: (480) 894-1600

Registration Form

Banquet Fees:

IEEE Members and Guests	$30.00
IEEE Student Members	$20.00
IEEE Student Member Guests	$30.00
IEEE Chapter / Society Table	$240.00*
Corporate Sponsorship	$500.00**

*Table sits 8 persons

**Sponsorship includes recognition at program, table of eight for dinner, and space for display

For additional information please access www.ieee.org/phoenix

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Please mail completed registration form along with your check, payable to: "**IEEE Phoenix Section**" and mail to:

Dr. Dongming He
Treasurer
IEEE Phoenix Section
437 East Tonto Place
Chandler, AZ 85249

Tel: **(480) 552-0947**
Fax: **(480) 552-1304**
Email: **dongming.he@intel.com (preferred)**

Banquet Timings:

Registration / Social Hour with Cash Bar:	6:00 PM – 7:00 PM
Dinner / Keynote Presentation:	7:00 PM – 8: 30 PM
Awards Program:	8:30 PM – 9:30 PM

Social Hour Hors D'Oeuvres:

Tequila Jalapeno Poppers
Teriyaki Beef Kabobs
Vegetable Tray with Ranch Dip
Crab Stuffed Mushrooms
Cheese and Cracker Tray

Cash Bar:

Sodas and Alcoholic beverages

Dinner Menu:

1) Petite Filet Mignon and Chicken Piccata Combo Dinner
2) Chilean Sea Bass Dinner
3) Vegetable Wellington with Roasted Red Pepper Sauce

Dinner Menu also includes Field Green Salad with Ranch and Vinaigrette Dressings, Garlic Mashed Potatoes, Rolls and Butter, Fresh Vegetables, Ice Tea and Water

Dessert:

New York Cheesecake with Strawberry Sauce
Coffee, Decaffeinated Coffee and Tea are served with Dessert

Please limit Registration to two persons per form, attach multiple forms if necessary. Detach below and mail with check.

IEEE PHOENIX SECTION ANNUAL BANQUET – 2006 Registration

(Please complete all sections of the form by typing or printing in bold and capital letters)

Name:

Guest Name:

Address:

Telephone Number: **Email:**

IEEE Member: **Yes** ☐ **No** ☐ **Student** ☐ **Membership #**

Dinner Choice (please select one per person)

(1) ___Petite Filet Mignon and Chicken Piccata Combo Dinner
(2) ___Chilean Sea Bass Dinner
(3) ___Vegetable Wellington with Roasted Red Pepper Sauce

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

An All Day Workshop

Memorial Union Building, Arizona State University, Tempe, Arizona

Thursday, November 10th, 2005

Submitted by Vasudeva P. Atluri, Ph.D., Workshop Chair and Charles E. Weitzel, Ph.D., Workshop Co-Chair

The IEEE Phoenix Section's Components, Packaging, and Manufacturing Technology Chapter with the Waves and Devices Chapter jointly held an all-day Workshop on Thursday, November 10th, 2005, at Arizona State University, Tempe, Arizona USA. The workshop was very well attended with about 196 registrants. The breakdown of registrants included 27 organizing committee members, 12 speakers, 22 vendor representatives, 72 IEEE members (including 5 student members), and 63 non-members (including 1 student). The workshop agenda included:

7:00 AM – 8:00 AM: Registration

7:50 AM – 8:00 AM: Introduction by Dr. Vasudeva P. Atluri, Intel Corporation, Chandler, Arizona. and Dr. Charles E. Weitzel, Freescale Semiconductor, Inc., Tempe, Arizona

8:00 AM – 9:45 AM: Morning Section I:

Chair: Mr. Mel Miller, Freescale Semiconductor, Inc., Tempe, Arizona.

- Topic 1: "*Keynote Presentation: Moore's Law Redux – Research in the Age of On-Chip, Converged Communication and Computing*", Presented by Dr. Krishnamurthy Soumyanath, Intel Corporation, Hillsboro, Oregon.
- Topic 2: "*A 2005 Perspective on MOSFET Scaling Challenges and Technology Innovations Through the End of the Roadmap*", Presented by Dr. Peter Zeitzoff, SEMATECH International, Austin, Texas.
- Topic 3: "*Advanced Devices for Future CMOS Nodes*", Presented by Dr. Suresh Venkatesan, Freescale Semiconductor, Inc., Tempe, Arizona.

9:45 AM – 10:00 AM: Refreshment Break / Vendor Displays

10:00 AM – 11:30 AM: Morning Session II:

Chair: Dr. Rashaunda Henderson, Freescale Semiconductor, Inc., Tempe, Arizona.

- Topic 4: "*Challenges for TCAD for Advanced Devices*", Presented by Dr. Mark Law, University of Florida, Gainesville, Florida.
- Topic 5: "*Opportunities and Challenges of III-Nitride Semiconductors*", Presented by Dr. Zlatko Sitar, North Carolina State University, Raleigh, North Carolina.
- Topic 6: "*Wireless Integrated MicroSystems (WIMS): Coming Revolution in the Gathering of Information*", Presented by Dr. Kensall Wise, University of Michigan, Ann Arbor, Michigan.

11:30 AM – 12:30 PM: Buffet Lunch / Vendor Displays

12:30 PM – 2:15 PM: Afternoon Session I:

Chair: Dr. Mali Mahalingam, Freescale Semiconductor, Inc., Tempe, Arizona.

- Topic 7: "*Flip Chip Packaging Technology for Next Generation Computing Applications*", Presented by Mr. Raj Master, Advanced Micro Devices, Santa Clara, California.

Topic 8: "*Future Decoupling Technology for High-Speed Integrated Circuits*", Presented by Dr. Richard Ulrich, University of Arkansas, Fayetville, Arkansas.

Topic 9: "*Electromagnetic and Circuit Co-Simulation – The Key to Next Generation Interconnect Design*", by Dr. Zoltan Cendes, Ansoft Corporation, Pittsburgh, Pennsylvania.

2:15 PM – 2:30 PM: Refreshment Break

2:30 PM – 4:00 PM: Afternoon Session II:

Chair: Dr. Ravi Sharma, Microchip Technology, Chandler, Arizona.

Topic 10: "*Hot-Spot Driven Thermal Management for Next Generation Computing and Communication Technology*", Presented by Dr. Avram Bar-Cohen, University of Maryland, College Park, Maryland.

Topic 11: "*Pb Free Interconnect – Industry Status & Trends*", Presented by Mr. Tim Olson, Mr. Ahmer Syed, and Mr. Jeff Cannis, Amkor Technology, Chandler, Arizona.

Topic 12: "*3D Integration Technologies – Motivation and Status*", Presented by Dr. Rajen Chanchani, Sandia National Laboratories, Albuquerque, New Mexico.

4:00 PM – 5:00 PM: Panel Discussion Titled "*Future of Computing and Communications*", Moderated by Dr. Stephen M. Goodnick, Arizona State University, Tempe, Arizona.

The morning session with a focus on Moore's Law Redux, A 2005 Perspective, Advanced Devices, Challenges, Opportunities and Future was very received by the workshop audience. Dr. Krishnamurthy Soumyanath suggested that the availability of low cost and power efficient MIPS (a direct consequence of Moore's law) makes ubiquitous mobile communications possible. The talk described a "digitally assisted analog" chip design methodology for on-chip, converged, communications and computations. Dr. Peter Zeitzoff summarized the overall scaling trends and issues for logic MOSFETs from the perspective of the 2005 International Technology Roadmap for Semiconductors (ITRS). Critical challenges with scaling include unacceptable increases in gate leakage current, increasing impact of polysilicon gate depletion, difficulty in obtaining adequate control of short channel effects, as well as others. Key technological innovations (referred to as "potential solutions" in the ITRS) to address these challenges include high-k gate dielectric, metal gate electrode, strained silicon channel to enhance the carrier mobility, and eventually, non-classical CMOS devices such as fully depleted, ultra-thin body, multiple-gate MOSFETs (e.g., FinFETs). Dr. Suresh Venkatesan covered the advanced device requirements and challenges for future CMOS nodes. With the non-scaling of gate oxides over the past few technology nodes, innovations in mobility scaling have been paramount to maintain performance requirements (different market segments having different power/performance operating points). Dr. Mark Law asserted that as Moore's Law drives device scaling, TCAD becomes both important and difficult. TCAD often becomes the only way to debug a problem or investigate an issue. His talk discussed modeling frameworks for making progress and covered recent experimental work that sheds light on the directions that need to be pursued for model development for future technologies. Dr. Zlatko Sitar indicated that unique properties of III-Nitrides (AlN, GaN, InN) make them superior for high power and high frequency applications. High current values in III-Nitride FETs can be combined with very high breakdown voltages, resulting in high power outputs. These devices have potential to replace traditional GaAs based microwave power FETs used in wireless communications. In his talk, a completely new approach was offered by the ability to grow controllably polar domains of different orientations side-by-side. These structures make use of the crystal polarity as a new degree of freedom for novel device structures that will be insensitive to surface charge. Dr. Ken Wise suggested that wireless integrated microsystems promise to become pervasive during the coming decade in applications ranging from health care and environmental monitoring to homeland security. Merging low-power embedded computing, wireless interfaces, and wafer-level packaging with microelectromechanical systems (MEMS), the resulting button-sized modules will serve as smart information-gathering nodes that will effectively wire the planet, extending communication networks to a wide range of new information-gathering applications. This talk highlighted two emerging microsystems – an implantable neural microsystem and a wristwatch-size environmental monitor.

The afternoon session focused on packaging technology, decoupling technology, electromagnetics and circuit simulations, thermal management, lead free, 3D integration, and panel discussion. Mr. Raj Master's talk included an overview of flip chip technology and challenges, package technology and manufacturability / design challenges, assembly technology and challenges, thermal issues and solutions, and overview / challenges of low K. Dr. Richard Ulrich explained that decoupling is the practice of bridging the power and ground planes of interconnect substrates with capacitors, which are distributed in location and value between the power supply and the IC. These caps provide the power to run the chip; the power supply just recharges the caps between clock cycles. The presentation reviewed the decoupling problem in general, the limits of using discrete capacitors, and the family of proposed future approaches that utilize embedded capacitance, including ferroelectric and paraelectric dielectrics, their possible inclusion into PWB's, their electrical performance and manufacturing issues. Dr. Zolton Cendes stated that engineers designing servers, storage devices, multimedia PCs, entertainment systems, and telecom systems that have driven an industry trend to replace legacy shared parallel buses with high-speed point-to-point serial buses. His talk presented a new reference design flow for high-speed serial interconnect simulation. The new flow included electromagnetic models for interconnects combined with advanced circuit simulation technology to model modern multi-gigabit transmission. Recent work on PCI Express backplane design, the Xilinx 10 Gb/s Backplane Design Kit, ultra-wideband radio design, and RFIC full chip extraction with on-chip spiral inductors was presented as application examples. Dr. Avram Bar-Cohen suggested that as Moore's Law progresses into the domain of nano-scale electronic, RF, and photonic features, steep increases in die heat flux and power dissipation results with the emergence of on-chip hot spots as the primary driver for advanced thermal packaging techniques. Following a brief review of the iNEMI thermal management roadmap for IC technology and the primary thermally-driven failure mechanisms, he talked about the thermal packaging "frontier" and the research required to address these emerging challenges. Mr. Tim Olson mentioned that with the July 1, 2006 European RoHS (Reduction of Hazardous Substances) directive deadline approaching, the electronic production supply chain is facing an unprecedented challenge in conversion to Pb free interconnect materials. His talk addressed the technical merits and existing concerns with respect to the implementation of the various RoHS compliant solutions. Dr. Rajen Chanchani provided an overview of 3D integration technologies including the motivation, description of the key technologies, and status of the technologies. The main motivating factors are 3D integration that enables miniaturization of Microsystems, a wider variety of technologies can be integrated with 3D integration, and electrical performance of 3D technology will be better. Various 3D technologies were described including issues associated with each category of technologies.

The day ended with an hour long panel discussion consisting of nine speakers and moderated by Dr. Stephen M. Goodnick. The topic was "Future of Computing and Communications". The panel discussion was interactive between speakers, audience, and moderator. The discussions among panelists and between panelists and audience were lively and interesting. About 40 people were in audience for the panel discussion.

The production of handouts and compact discs as well as breakfast, refreshment breaks, and lunch were subsidized in part by the financial support obtained from the Premier Sponsors who contributed $1000 and Standard Sponsors who contributed up to $500. The Premier Sponsors included Freescale Semiconductor, Inc., IEEE Phoenix Section, and Intel Corporation. The Standard Sponsors included Arizona State University Department of Electrical Engineering and Connection One Center, IEEE Antennas and Propagation Society, IEEE Components, Packaging, and Manufacturing Technology Society, IEEE Microwave Theory and Techniques Society, Motorola, Inc. and RF Micro Devices. Premier sponsor Freescale Semiconductor, Inc. had a display that was very well received. Many of workshop attendees, including both IEEE and non-IEEE members, stopped by the IEEE display and benefited by the information that included local chapters missions, literature, and membership forms. The display in general sparked considerable interest among IEEE non-members to join IEEE.

Total of 18 vendors had displays at the workshop. Vendors included 3M Electronics, Advanced Packaging & Systems Technology Laboratories, LLC., Ameriprise Financial Services, Ansoft Corporation, Cadence Design Systems, CMC Interconnect Technologies, Fluent, Inc., GE Silicones, Jacket Micro Devices, Namics Technologies, Inc., Optimal Corporation, Phoenix Analysis & Design Technologies, Rogers Corporation, SONNET Software, Tango Systems, Inc., Techsearch International, Inc., Tektronix, Inc., and Zeland Software, Inc. These displays were very professionally done, technically oriented, and contributed to the overall success of the workshop. The workshop only had space only for a total of 18 vendors and was not able to accommodate other requests. There was an increase of one vendor display over last year's workshop.

The workshop was made possible by the hard work of the organizing committee consisting of members from both IEEE Phoenix Section CPMT Chapter as well as WAD Chapter. Long hours of dedicated work over a period of nine months by all members of the workshop organizing committee contributed to the overall success of the workshop. The workshop organizing committee consisted of the following members:

General Chair:	Vasudeva P. Atluri, Ph.D.		Sam Karikalan
Co-Chair:	Charles E. Weitzel, Ph.D.		Steve Rockwell
Technical Program:	Mali Mahalingam, Ph.D.	Electronic Media:	James E. Drye
	Mel Miller		Samir Pandey, Ph.D.
	Rao Bonda, Ph.D.	Registration:	Monica C De Baca
	Henning Braunisch, Ph.D.		Vivek Gupta
	Bishnu Gogoi, Ph.D.		Vladimir Noveski, Ph.D.
	Stephen Goodnick, Ph.D.		Sergio Pacheco, Ph.D.
	Rashaunda Henderson, Ph.D.	Arrangements:	Ankur Agrawal, Ph.D.
	Sujit Sharan, Ph.D.		Shane Johnson, Ph.D.
	Ravi Sharma, Ph.D.		Margaret Szymanowski
	Dragan Zupac, Ph.D.	Publicity:	Craig Birtcher
Vendor Registration:	Bruce Bosco		Steve Post
	Eric C. Palmer		

By bringing renowned speakers to address the most relevant topics, the workshop once again provided an excellent learning opportunity for professionals in valley. In addition to raising funds for IEEE Phoenix Section CPMT chapter and WAD chapter, one of the goals of the workshop is to help increase the IEEE Phoenix Section Scholarship Endowment at Arizona State University Foundation. Continuing with the tradition from previous three years, 50% of the profits were donated to the Endowment. This year $11,000.00 were donated bringing the total contributions from the last four workshops to about $28,000.00. This endowment is helping IEEE Phoenix Section give awards to undergraduate IEEE student members within IEEE Phoenix Section region. Students from Arizona State University, Devry Institute, Embry-Riddle Aeronautical University, and Northern Arizona State University are eligible to apply for these scholarships. The scholarship fund was originally initiated jointly by IEEE Phoenix Section, IEEE CPMT Phoenix Chapter, and IEEE WAD Phoenix Chapter.

Picture of organizing committee members and volunteers in front of IEEE Phoenix Section display at the workshop