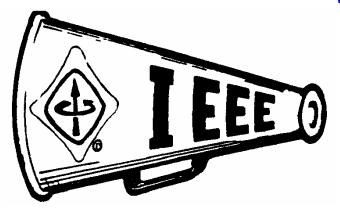
# The Valley Megaphone



# Newsletter of the Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

August 2007, Volume XXI, Number 8

# **Executive Committee**

# **Past Chair**

Rao Thallam, 602-236-8064 thallam@ieee.org

### Chair

Rao Bonda, 480-413-6121 r.bonda@ieee.org

### Vice Chair

Dongming He, 480-552-0947 dongming@ieee.org

### Secretary

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# Treasurer

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Jim Drye, 480-413-5685 jdrye@ieee.org

## Conferences

Henning Braunisch, 480-552-0844 braunisch@ieee.org

# Awards

Vasudeva P. Atluri, 480-554-0360 vpatluri@ieee.org

# Inter-Society

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## Web Master

Chandan K. Das, 480-554-1300 cdas@ieee.org

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IEEE Phoenix Section Executive Committee meeting minutes can be found at: <a href="http://www.ieee.org/phoenix">http://www.ieee.org/phoenix</a>

Please send announcements for Valley Megaphone to Eric Palmer: <a href="mailto:ecpalmer@ieee.org">ecpalmer@ieee.org</a>.

# **Chapters**

Communication & Signal Processing
Gang Qian
gang.qian@asu.edu

### **Computer Society**

Cesar A. Vasquez-Carrera C. Vasquez-Carrera@computer.org

# Consultants Network (PACN)

Vaughn L. Treude, 602-750-3662 vaughn@nakota-software.com

# **CPMT Society**

Victor Prokofiev victor.prokofiev@intel.com

# **Education Chapter**

Martin Reisslein, 480-965-8593 reisslein@asu.edu

# **EMBS Chapter**

Ahmed Abdelkhalek ahmed\_a@acm.org

# **EMC Society**

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# GOLD

Mike Poggie

Mike.Poggie@ieee.org

# Power Engineering Society Jim Hudson

jhhudson@srpnet.com

# **Solid State Circuits**

Bertan Bakkaloglu bertan@asu.edu

# **Waves & Devices Society**

Chuck Weitzel, 480-413-5906 Chuck weitzel@freescale.com

The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.

Advertising Rates: Full page: \$200, 3/4page: \$125, ½ page: \$75, 1/3 page: \$50, 1/4 page: \$25.

Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

# **Student Branches**

ASU Main, Engineering

Chair: Cory P. Murphy ieeeasuchair@gmail.com Advisor: Cihan Tepedelenlioglu, (480) 965-6623, Cihan@asu.edu

ASU Main, Computer Society

Chair: Luis Tari luis.tari@asu.edu

Advisor: Joseph Urban, 480-965-3374, joseph.urban@asu.edu

ASU Polytechnic

Chair: Brian Siskoy bsiskoy@gmail.com Advisor: Barbara Rempel Barbara.Rempel@asu.edu

**DeVry, Phoenix** Chair: Richard Taylor

RLTaylor@ieee.org

DeVry, Computer Society

Chair:

NAU, Engineering Chair:

Advisor: Phil Mlsna, 928-523-2112 Phillip.Mlsna@nau.edu

Embry-Riddle, Prescott

Chair: Advisor: Chuck Cone conec@erau.edu

Tuesday of the month.

**Time:** 6:00 pm to 8:30 pm

Place: Phoenix Airport Hilton, 2435 South 47th Street

Phoenix, AZ, 85034 Phone: 480-804-6017

**Directions:** From 143, exit University Ave, go west, turn right on 47<sup>th</sup>

**Phoenix Section Executive Committee Meeting – First** 

street.

**More Info:** Meetings held first Tuesday of month. No meetings in July

and August. All interested IEEE members are welcome to

attend.

Contact: Rao Thallam, Phoenix Section Chairman, ph. (602) 236-5481

or e-mail: thallam@ieee.org

<advertisement>

# **Instructors Needed Now for Fall Semester:**

Instructors needed in:

Electrical Math

Electrical

Computer Electronics

Positions available:

Evenings & Part-Time Phoenix Metro Area

Fax or email your resume to:

Yolanda Price

Director of Education

602-277-9881 (fax)

yprice@electricleagueofarizona.org

The Electric League of Arizona Founded 1960



# 2007 IEEE-USA Annual Meeting Technical Workshops 31 August 2007



The Phoenician Resort, Scottsdale, AZ http://thephoenician.com/pages/index.html

Stay competitive through hands-on training and in-depth presentations. Meet industry experts. Share ideas and learn. Join us for technical workshops at the 2007 IEEE-USA Annual Meeting where you will participate in hands-on training highlighting some of the latest technologies. All attendees will receive a certificate for 7 PDHs.

# Registration 7:00 - 8:00 am

Disaster Recovery	LabVIEW	Rational	Emerging Technology
Disaster Recovery	LabVIEW & Computer-Based	Modern Software Best	Technologies, Tools &
Vishnu Pandey - HP	Measurements	Practices & Techniques	Instructional Resources
	Doug Kunz & Michael Bryner - NI	Anthony Crane - IBM	John McLellan - Freescale
Keynote Luncheon - Technology Challenges Facing Engineering to Meet Cost & Performance			
Dr. Gaurang Choksi, Manager, Intel Core Competency Group			
Disaster Recovery	LabVIEW RealTime	Modern Software Best	RFID Technology Seminar
Vishnu Pandey - HP	Doug Kunz & Michael Bryner - NI	Practices & Techniques	Emily Sopensky - IEEE
		Anthony Crane - IBM	Kristin Hedger & Gene Fedors
			Virtual Training Environment Jim Wrubel - SEI

# Course Information:

**Disaster Recovery:** Need data availability 24/7? An overview of Storage Area Networks (SANs), followed by in-depth discussion of architecting a fully-redundant solution that provides the best protection for your data.

**LabVIEW and Computer-Based Measurements Hands-On:** Learn how to build measurement and control applications through practical examples using National Instruments LabVIEW graphical programming.

**LabVIEW RealTime:** Learn how to design real-time, deterministic data acquisition and control applications.

Modern Software Best Practices & Techniques: Learn essentials of iterative development with Rational Unified Process, requirements management in an iterative lifecycle, successful use cases and enabling Portfolio Management.

**Technologies, Tools & Instructional Resources:** A demonstration of learning environments, student educational kits, and accompanying lab modules designed for industry, educational institutions and hobbyists. Freescale Semiconductor will present their broad portfolio of technologies, innovative products, and services.

**RFID Technology:** Emily Sopensky, The Iris Company, Kristin Hedger, Killdeer Mountain Manufacturing, and Gene Fedors, RFID Technical Institute, will present an introduction to RFID technology and its applications.

**SEI's Virtual training Environment:** High-fidelity Web-based training using video and hands-on labs. This presentation will describe the key technologies used in VTE, demonstrate the application, and offer lessons learned.

Workshop Registration Fee (before July 15)\* Workshop Registration Fee (after July 15) Includes keynote luncheon Includes keynote luncheon Student/Life Member Student/Life Member \$55 \$60 **IEEE Member** \$150 **IEEE Member** \$195 IEEE Non-Member \$200 IEEE Non-Member \$250

# Attendee Registration available on-line at

http://www.ieeeusa.org/calendar/conferences/2007annualmeeting/registration/default.asp

\*Corporate discount - 5 conference attendees for \$600, Contact Linda Hall at l.hall@ieee.org for corporate registration.

**Platinum Sponsors:** 





















# Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter

Waves and Devices Chapter PRESENT AN ALL-DAY WORKSHOP ON

# **Emerging Device and Packaging Technologies**

Date: Friday, November 9<sup>th</sup>, 2007 Time: 7:00 A.M. – 5:00 P.M.

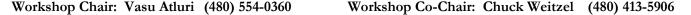
Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

# **Abstract**

The semiconductor industry is entering an era with tremendous opportunities to exploit emerging technologies for the benefit of widely diverse markets. Moore's Law requires increasingly intensive materials innovations to maintain its momentum. Meanwhile, new markets in the areas of bioelectronics, sensors, etc., are leveraging the existing manufacturing infrastructure while incorporating new materials and techniques. This one-day workshop will bring together experts from industry, academia, research labs, and consortia to share their technology roadmaps and visions, novel materials and methods, and discuss technical opportunities. The status and challenges facing device, interconnect, and packaging technologies will be discussed in depth. An expert panel discussion will bring a closure to the day's workshop. Vendors will be on hand to exhibit products and services in all aspects of the supply chain for IC, packaging, and module design and manufacturing.

# **Topics**

- Nanotechnology and Continuum Model Limits
- ITRS Roadmap Challenges
- SiP: 3D, Modules, Discrete Passives Integration
- Flexible Electronics
- Green Materials and Packaging
- Bioelectronics and Sensors Technologies
- General Industry and Technology Visions
- Panel Discussion on Future Challenges and Opportunities for Emerging Technologies





For General Information: For Workshop Sergip Pacheco For Vendor Vladimir Noveski http://www.ieee.org/phoenix Registration Forms: (480) 413-3737 Registration Forms: (480) 554-2375

# INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS



# WAVES AND DEVICES PHOENIX CHAPTER

August 6, 2007 www.eas.asu.edu/~wadweb



# Electrostatic Discharge (ESD) Protection for RF IC's Juin J. Liou

Professor, Dept. of Electrical and Computer Engineering Director, Solid State Electronics Lab and Device Characterization Lab University of Central Florida, Orlando, Florida, USA

# **Abstract**

Electrostatic discharge (ESD) is a process in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and more than 35% of chip damages can be attributed to such an event. As such, designing robust on-chip ESD structures to protect microchips against ESD stress is a high priority in the semiconductor industry. An overview on the ESD sources, models, and protection schemes will first be given in this talk. This is followed by the development of a procedure to optimize the ESD structures for optimal robustness and minimal parasitic capacitance for RF applications.

# **Biography**

**Juin J. Liou** received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida where he is now a Professor. His current research interests are Micro/nanoelectronics computer-aided design, RF device modeling and simulation, and electrostatic discharge (ESD) protection design and simulation.

Dr. Liou has filed 3 patents, and has published 6 textbooks (another in progress), more than 210 journal papers (including 13 invited articles), and more than 160 papers (including 58 keynote or invited papers) in international and national conference proceedings. He has been awarded more than \$7.0 million of research contracts and grants from federal agencies (i.e., NSF, DARPA, Navy, Air Force, NIST), state government, and industry (i.e., Semiconductor Research Corp., Intel Corp., Intersil Corp., Lucent Technologies, Alcatel Space, Conexant Systems, Texas Instruments, Fairchild Semiconductor, Analog Devices, RF Micro Device, Lockheed Martin), and has held consulting positions with research laboratories and companies in the United States, China, Japan, Taiwan, and Singapore.

Dr. Liou received ten different awards on excellence in teaching and research from the University of Central Florida (UCF) and six different awards from the IEEE Electron Device Society (EDS). Among them, he was awarded the UCF Distinguished Researcher Award three times (1992, 1998, 2002), UCF Research Incentive Award two times (2000, 2005), and IEEE Joseph M. Biedenbach Outstanding Educator Award in 2004 for his exemplary teaching, research, and international collaboration. His other honors include Fellow of the IEE, Trustee Chair Professor of UCF, Cao Guang-Biao Endowed Professor of Zhejiang University, China, Consultant Professor of Huazhong University of Science and Technology, Wuhan, China, Courtesy Professor of Shanghai Jiao Tong University, Shanghai, China, IEEE EDS Distinguished Lecturer, and National Science Council Distinguished Lecturer.

Date: Monday, August 6, 2007

<u>Location</u>: Bernoulli Conference Rm, Bldg 99, Freescale Semiconductor, 2100 E. Elliot Rd., Tempe Drive North on Country Club off Elliot on the western edge of the Freescale site, enter back parking lot

**Time**: 3:30 - 5:00pm Presentation

For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906

# INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS



# COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY ECTC Components & RF Program Committee CPMT RF & Wireless Technical Committee



58th ECTC May 27 – May 30, 2008 Orlando, Florida USA

The CPMT RF & Wireless Technical Committee and the ECTC Electronic Components & RF Program Committee encourage you to submit an abstract to ECTC 2008 in the area of passive components & networks, RF and Microwave components and modules and subsystems. ECTC is the premier Electronic Components and Packaging conference held annually and attended by about 1000 delegates with equal participation from companies and academia. As in the past, Components, RF & Microwave related papers are solicited for focus sessions during this prestigious conference.

# **Discrete Passive Components**

Design, materials, processes and manufacturing considerations for discrete passive components- resistors, capacitors, inductors and passive networks.

# **Integrated and Embedded Passive Components**

Design, materials, processing, modeling, manufacturing, and characterization of integrated and embedded passive components on silicon, organic, ceramic and glass type substrates for digital, mixed signal, & RF applications

# Materials, Processing, Reliability, and Manufacturing of Electronic Components

Design, Materials, Processing, yield and reliability aspects of electronic components

# **New Technology Development for Electronic Components**

Technologies for on chip integration of passive components – silicon through vias, wafer level RDL, nano materials and processes

Technologies for substrate level integration – embedded passive and active components, component integration on ultra thin substrates

# **RF** and Microwave Components

Integrated antennas, filters, baluns, RFID/sensors, RF MEMS, tunable devices and switches, high power and high efficiency RF/Microwave power amplifiers- design, technology and high frequency characterization

# **RF and Microwave Modules**

Module Integration technologies in semiconductor, organic and glass substrates – System in Package, System on Chip, Package on Package, 3D integration

# **SUBMISSIONS:**

Please submit abstracts using the ECTC web site: <a href="www.ectc.net">www.ectc.net</a> by October 15, 2007. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Components & RF" focused sessions YOU MUST SELECT "Electronic Components & RF" committee as your PRIMARY subcommittee preference when you submit your abstract at the ECTC web site. Again, to have your paper considered for the RF & microwave components sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site (<u>www.ectc.net</u>) and select <u>"Electronic Components & Daniel Date of the ECTC web site (www.ectc.net</u>)

RF" as PRIMARY subcommittee preference

STEP #2: Email abstract copy and author's email & contact information to: Craig Gaw at c.a.gaw@ieee.org &

Mahadevan Iyer at mahadevan.iyer@ece.gatech.edu

Craig Gaw, Chair - CPMT RF & Wireless TC Freescale Semiconductor Inc.

c.a.gaw@ieee.org

Mahadevan K Iyer, Chair - ECTC RF & Components TC Georgia Institute of Technology

mahadevan.iyer@ece.gatech.edu



# THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.



# IEEE Components, Packaging and Manufacturing Technology Society Phoenix Chapter

Wednesday, August 15th, 2007 Meeting

# Enabling 300mm IC Manufacturing Using Advance Factory Automation

# Dev Pillai Intel Fellow Director, Operational Decision Support Technology

Logic Technology Development Automation Group Intel Corporation Chandler, Arizona

# **Abstract**

The talk will describe key elements of Intel's Factory Automation systems that enable many millions of leading-edge products to be ramped at very high yields in multiple factories in a very short time. These include fully automated operations which have been deployed pervasively that enable operational and engineering innovations, and automated process & tool matching capabilities that result in the manufacturing of identical products from different factories. The talk will also discuss use of common platforms for rapid automation solutions deployment across the manufacturing chain, and cover the use of mathematical optimization, simulation modeling and machine learning techniques that are used extensively to optimize the manufacturing networks.

# **Biography**

Dev Pillai is Intel Fellow and Director of Operational Decision Support Technology in Intel's Logic Technology Development group. His team play pivotal roles in the development and proliferation of dynamic factory modeling, factory integration, and mathematical optimization techniques across Intel's wafer fabrication, sort, assembly and test factories. Prior to his current position, Dev led Intel's highly successful 300mm factory integration efforts that resulted in production equipment, automation systems and wafer fab standardization that had never been achieved before. He has been honored many times by his industry peers as one of the most influential engineers who drove the vision and industry direction for large-scale factory automation in semiconductor manufacturing.

Dev has published over 90 technical papers in IEEE, ISSM, SME, JES, IIE and SEMI publications on advanced manufacturing topics. He has a BS in mechanical engineering from National Institute of Technology, Calicut, India and MSIE specializing in computer aided processes from Arizona State University.

**Date:** Wednesday, August 15<sup>th</sup>, 2007

Location: Group Conference Room, Freescale Semiconductor, Inc., 2100 E. Elliot Rd. Tempe, Arizona

Enter the facility through the Main (South) lobby, by the flag poles; you will be escorted to the meeting venue.

Time: 5:30-6:00 Social/Refreshments, 6:00-7:00 Presentation, 7:00 Dinner

(Pizza and Soda are being provided by the IEEE CPMT Phoenix Chapter)

IEEE members and non-members all are welcome to attend. Those who plan to attend should be at the facility entrance no later than 6:00 pm, as there will be no escorts available after that.

# For more information please call any of the following officers:

Debendra Mallik (480) 554-5328 Vasu Atluri (480) 554-0360 Samir Pandey (480) 552-7502 Vivek Gupta (480) 413-5849 Mali Mahalingam (480) 413-5368 Rao Bonda (480) 413-6121 Victor Prokofiev (480) 552-0228 Qing Zhou (480) 552-9177 Jim Drye (480) 650-8826

# **IEEE Mentoring Connection**

IEEE is offering its members the opportunity to participate in an online program which will facilitate the matching of IEEE members for the purpose of establishing a mentoring partnership. By volunteering as a mentor, individuals use their career and life experiences to help other IEEE members in their professional development. I believe this program can be a great tool to provide our newest members of our profession guidance in their careers and provide experienced members a chance to hear first hand from the newly graduated about the latest training the next generation is receiving. This is a program for higher level members and is provided to help ease the transition out of school and into a career.

As a mentee, you lead your partnership by selecting your mentoring partner from among those who have volunteered to serve in this capacity. I ask that you review the time and effort commitment to the program to ensure a successful mentoring partnership. Participation in the program is voluntary and open to all IEEE members above the grade of Student Member.

If you are interested, please go to <a href="http://www.ieee.org/mentoring">http://www.ieee.org/mentoring</a> for information on the roles and responsibilities of each mentoring partner. I encourage you to take advantage of the IEEE network of technical professionals or offer your expertise and sign up for the online mentoring program today.

### Who can be an IEEE Mentor?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Able to communicate effectively with others
- Willing to share some career successes and failures
- Individuals who may be or have been executives, consultants, or in middle or upper management, or in research
- Individuals who may be or have been educators, entrepreneurs, or self-employed
- Individuals who may be or have been proven leaders offering inspiration and insight
- Individuals who may be or have been IEEE officers or volunteers
- Willing to review an orientation session to learn guidelines, tools of program and the mentee and mentor's role and responsibilities

# Who can be an IEEE Mentee?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- New professionals in their first or second job, or considering entering graduate programs
- Recent graduates entering the professional workforce for the first time
- Professional making a career move or career change
- Passionate for learning
- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Willing to identify and clarify their developmental goals
- Interested in learning from another professional "who has been there"
- Willing to participate in mentee orientation session to learn guidelines, and tools of program and their role and responsibilities as a mentee

This program deserves your consideration and doesn't require a large amount of time on your part. It can provide of great assistance to the next generation of engineers.

Russ Kinner Membership Chair, Phoenix Section

# **RE-SEED**

# Retirees Enhancing Science Education through Experiments & Demonstrations

# **Overview**

RE-SEED (Retirees Enhancing Science Education through Experiments and Demonstrations) is a Northeastern University program that prepares engineers, scientists, and other individuals with science backgrounds to work as volunteers, providing in-classroom support to upper elementary and middle school science teachers with teaching the physical sciences.

After completing a comprehensive free training program, participants volunteer in middle school classrooms on the average once a week for at least one year. RE-SEED began in 1991 with six volunteers. To date close to 500 RE-SEED volunteers have worked in schools in about 100 communities throughout the country offering about 500,000 hours of their time.

Nationally, 75 percent of 7th and 8th grade students are taught physical science by teachers who do not have a major or a minor in the subject (The National Science Board, Science and Engineering Indicators 2000). RE-SEED volunteers possess talent and expertise that complement those of science teachers. They bring with them a wealth of knowledge and experience that allows them to make science interesting and relevant to everyday situations.

RE-SEED volunteers work closely with the host science teachers to help them enrich and implement their school curriculum. Overall the volunteers become involved members of their schools' and even their districts' teaching team, sometimes taking part in curriculum adoption decisions.

Please contact us by email at <a href="mailto:reseed@neu.edu">reseed@neu.edu</a> or phone 888-742-2424; Shelia Kirsch at <a href="mailto:Sheila.Kirsch@asu.edu">Sheila.Kirsch@asu.edu</a> and / or Deirdre Weedon, <a href="mailto:d.weedon@neu.edu">d.weedon@neu.edu</a>. if you are interested in learning more about these training programs.