The Valley Megaphone

Newsletter of the
Institute of Electrical and Electronics Engineers, Inc.
Phoenix Section
April 2007, Volume XXI, Number 4

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Contents:

IEEE Phoenix Section Executive Committee meeting minutes can be found at: http://www.ieee.org/phoenix

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.
Advertising Rates: Full page: $200, 3/4page: $125, ½ page: $75, 1/3 page: $50, 1/4 page: $25.
Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

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Embry-Riddle, Prescott
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Advisor: Chuck Cone
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Phoenix Section Executive Committee Meeting – First Tuesday of the month.

Time: 6:00 pm to 8:30 pm

Place: Phoenix Airport Hilton, 2435 South 47th Street
Phoenix, AZ, 85034
Phone: 480-804-6017

Directions: From 143, exit University Ave, go west, turn right on 47th street.

More Info: Meetings held first Tuesday of month. No meetings in July and August. All interested IEEE members are welcome to attend.

Contact: Rao Thallam, Phoenix Section Chairman, ph: (602) 236-5481 or e-mail: thallam@ieee.org

Special Presentation by Russell Harrison, IEEE-USA Legislative Affairs, Grassroots Initiative Coordinator

On **Tuesday, April 3 from 4:30-5:30**, Russell Harrison will be speaking at the **Airport Hilton**, 2435 S. 47th Street. This presentation is open to all members and any other interested individuals.

Presentation Summary

Every year our elected officials make thousands of decisions that require an understanding of science or technology - despite the fact that most of our elected officials don't understand either science or technology.

Legislatures move so fast that few elected officials have the time to seek out the information they need before making decisions. Rather, politicians listen to whomever talks to them, and then make the best decision they can. If they are lucky, one of the people who is talking to them will be an engineer.

Russell will discuss current legislation before Congress that will impact engineers and their careers.
Then, he'll discuss proven strategies used by engineers to communicate with legislators.

Congress is interested in hearing from engineers and scientists. But if we don't speak up, they aren't going to come to us. Join us for an evening to discuss how to help elected officials better understand us, what we do and how what they do impacts us.

Advanced Materials/Failure Analysis (AMFA) Workshop

April 20, 2007 • Hyatt Regency Hotel • Phoenix, Arizona

***AMFA MISSION**:*

*To serve the interests of failure analysis & materials characterization professionals by providing a forum for the presentation and **active** discussion of timely and pertinent technological issues and trends and to promote the development of new capabilities that fill critical gaps in emerging technologies.*

Unlike traditional conferences that often restrict audience participation, AMFA Workshops provide only top quality invited speakers on leading edge topics, in a format where audience participation is expected and strongly encouraged.

Program

•*Leveraging Federal Funding for Characterization Tools*…….Bruce Gnade, University of Texas, Dallas

This presentation will address funding schemes to develop sophisticated, small volume analytical tools for the semiconductor industry. History has shown us that development cycles of 5-7 yrs and millions of dollars of non-refundable engineering costs are typical. The problem is exacerbated by small world wide sales and the fact that typically the tools are being developed by small, venture capital firms whose budgets are strained. The presentation will include an introduction based on the actual development costs and resources necessary to bring x-ray tomography to the marketplace and the path forward to avoid some of the obvious limitations of that process.

•*"FA Role: Dynamic Driver or Passive Passenger?"*..Rich Blish, Spansion; Efrat Raz, Gemtech

The FA team does not take an active role in technology roadmaps, design reviews, production assessment and post analysis recovery plans and with a limited budget it is expected to continue to support advanced technology and production cost cutting - crying silently in our beer won't change anything! We must demand to become a *technical* partner by developing interactive communication; demanding data and being a follow up partner. The FA manager must be a *business* manager, who markets his/her products aggressively. Success must be communicated both technically and in dollar terms - "top management language".

•*"FA Role: Dynamic Driver or Passive Passenger?"*……..Breakout Discussion

Metrology for Emerging Devices and Materials ……Eric Vogel, University of Texas, Dallas
Scaling of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and its traditional materials has been the basis of the semiconductor industry for nearly 30 years. A wide variety of materials and devices are emerging to extend and replace the traditional MOSFET. This talk will provide an overview of these emerging devices and materials and of the metrology requirements for these technologies

Atomic Level Ion Source Microscopy. . . . . .Bill Ward, ALIS Corp.
A novel helium ion microscope has been developed which has advantages over traditional scanning electron microscopes(SEMs) and focused ion beams (FIBs) for many applications. The ALIS scanning ion microscope uses a beam of helium ions as the imaging particles. Ions can be focused into a smaller probe size - less than 1 nm with a properly designed column, and have less sample interaction than electrons. The ALIS microscope can generate higher resolution images with more material contrast so more detail can be seen. We expect to be able to see things much smaller than we've ever been able to see with even the most sophisticated scanning electron microscope (SEM).

Materials Characterization Using Ultrafast Lasers……...David Cahill, University of Illinois
This presentation describes how the rapid heating of the near surface of metal films by nJ ultrafast optical pulses can be used to generate nanoscale wavelength strain and temperature fields for measurements of the mechanical and thermal properties of thin films and interfaces.

Failure Analysis Year In Review……Christian Boit, Berlin University of Technology
FA innovation trends are measured by IC technology roadmaps. This presentation takes snapshots of the year and introduces major trends. A picture of the dynamics in the different analysis sections metrology, debug/diagnosis on die and package and their respective interactive potential emerges that also anticipates economical aspects of the development.

Registration Fees: $150.00 for IEEE or EDFAS members, $200.00 for non-members. Registration may be done online at www.amfaworkshop.org (after Jan. 01), onsite during IRPS, or at the AMFA Workshop. Registration for the AMFA Workshop includes a CD-ROM of the presented materials, lunch, and morning/afternoon breaks.

The AMFA Workshop is technically co-sponsored by the IEEE Reliability Society and the Electronic Device Failure Analysis Society.

For general workshop information, visit http://www.amfaworkshop.org/ or contact:

Gay Samuelson
Workshop Chair, AMFA
Technical Consultant
Tel: (480) 707-2083
Email: g.m.samuelson@att.net

For registration and mailings
IRPS Publishing Services
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Fax: (315) 336-9134
e-mail: pub_services@irps.org

Semitracks, Inc. is proud to bring three unique courses to the Phoenix area in April.

Packaging Technology/Challenges
Instructor: Dr. Gay Samuelson
April 9-10, 2007

This course provides an overview of the current business climate, anticipated trends and the associated impact on assembly/packaging.
Topics include the following:

- In depth discussion of several roadmaps and their impact on packaging.
- Assembly flows and cost implications for wafer fabrication and assembly with special focus on low cost alternatives.
- Reliability issues, such as thin film delamination/cracking, bump cracks, via delamination/ cracking, thermal interface degradation, heat sink retention, and socketing issues
- Failure analysis tools, such as SAM, x-ray, SQUID microscopy, TDR, terahertz imaging, thin film materials characterization, and adhesion testing.
- Impact of the latest technologies such as Cu, ultra low k dielectrics, 300mm wafer fabrication, wafer scale packaging, embedded passives, chip on board, and modular integration.
- Future packaging needs for MEMS, and Nanotechnology.

This course is recommended for engineers and scientists involved in the rapidly expanding arena of assembly/packaging in the digital revolution. This course will also be useful to engineers and scientists performing risk assessments on packaging technologies, fault isolation and failure analysis and stress testing to achieve reliability certification of such technologies.

Package Design and Modeling
Instructor: Mr. Steve Groothuis
April 11-13, 2007

This course provides an introduction to assembly/packaging design and modeling process as well as a variety of design and simulation tools used on current technologies.
This class focuses on techniques and the importance of thermal and mechanical simulations. Discussions and examples will concentrate on thermal performance simulations, assembly & packaging stresses, package reliability (including solder joint fatigue simulation), and interactions between chip and package. In addition, a special section will be examples of successful wafer level simulations.
The course covers:

- Current packaging technologies, including chip scale packaging, Ball Grid Array technology and other current concepts.
- Thermal simulations, including modeling power dissipation and thermal diffusivity.
- Mechanical simulations, including thermomechanical interactions and materials thermal coefficient of expansion mismatches.
- Soldering stresses
- Reliability and failure mechanisms
- Package/die interactions
- Wafer level simulations that impact packaging.

This course is recommended for engineers and scientists involved in the design and modeling of packages and package materials, engineers working package/assembly-wafer manufacturing interactions, and reliability engineers.

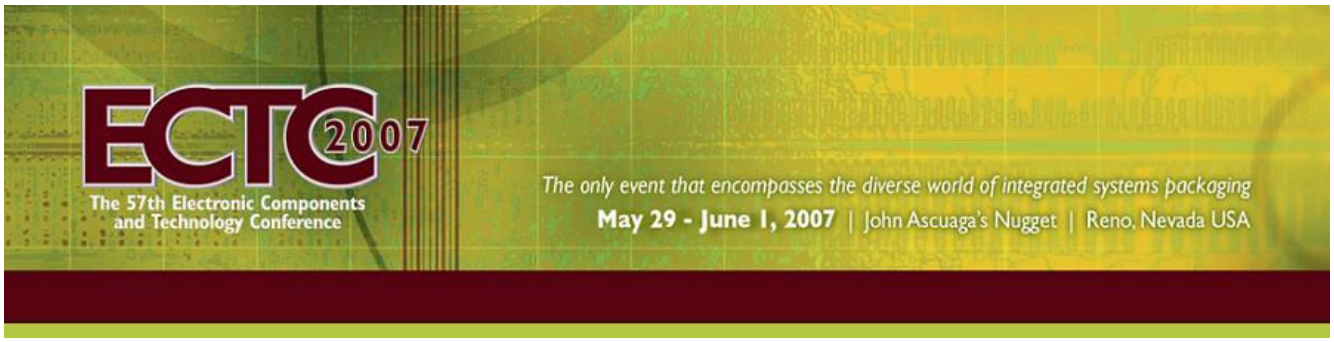
ESD/Latchup Design & Technology
Instructor: Dr. Steven Voldman
April 12-13, 2007

This course provides an in-depth look at the art and science behind ESD and Latchup Design and Fabrication technology.
Electrostatic Discharge (ESD) and Latchup are a critical concern for the semiconductor and electronics industry. Both ESD and Latchup account for more than $4 Billion in losses each year. This problem is likely to grow in the future as smaller feature sizes are susceptible to damage at lower static voltages and latchup under more subtle conditions.
This course covers:

- Fundamentals and current issues in latchup
- Latchup physics, test structures, characterization, process and technology issues, and new latchup issues in the industry today.
- Fundamentals of ESD. The instructor will first give a background tutorial on ESD physics, electro-thermal and statistical models.
- CMOS, silicon on insulator (SOI) and silicon germanium (SiGe) technologies
- ESD devices, circuits, and process issues in RF CMOS, RF BiCMOS silicon germanium technologies, and gallium arsenide (GaAs).

Participants will also receive copies of Dr. Voldman's books *ESD: Physics and Devices*, and ESD: Circuits and Devices.
This course is recommended for ESD designers, product engineers, reliability engineers, and device technologists.

All three courses will be held at the Hampton Inn and Suites Phoenix/Tempe, 1429 North Scottsdale Road, Tempe AZ, United States, 85281. Tel. 480-675-9799. For more information, or to register for the courses, please visit our website at http://www.semitracks.com/courses/phoenix-courses.htm or call us at 505-858-0454.
Please forward this announcement to colleagues who might be interested.



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IEEE Grows Membership in 2006

From Russ Kinner, Membership Development Chairman

In 2006, IEEE grew its membership by 2%, to a total of 374,767 members. Both higher-grade and student grade membership surpassed 2005 year-end results, driven by gains in five Regions—3, 7, 8, 9, and 10 (southeast US and the rest of the world).

At the close of the year, Region 10 (Asia) is IEEE's largest region with 67,442 members. Region 8 is second, with 60,856 members. Reversing a four-year trend, total **higher-grade membership** exceeded 2005. At the close of the year, IEEE had 294,276 higher-grade members, 751 more than last year. Positive results were driven by gains in four Regions—5, 7, 8, and 9.

Student membership in IEEE established a new record in 2006. At the close of the year, the IEEE had 80,491 student members. This represents growth of 9% over last year's all-time high of 73,870. The strong results were driven by gains in five Regions—1, 3, 7, 8, and 10.

Society memberships ended the year down by 2.5%, an aggregate loss of 8,777 memberships. At the close of the year, the Computer Society (CS) was the largest Society with 86,057 members. The Communications Society (COM) was the second largest with 41,016 members.

Locally the Phoenix section has 3472 total active members with 812 members who have not yet renewed their memberships as of March 18. Region 6 (where Phoenix is located) lost 532 higher grade members and 199 Students for 2006 to drop into 3rd place among the 10 regions of the IEEE.

	Higher Grade Members		Change	Total Members		Change
Region	**2006**	**2005**	**#**	**2006**	**2005**	**#**
6	**53670**	**54202**	**-532**	**60,139**	**60,870**	**-731**
USA	**188745**	**190878**	**-2,133**	**215,851**	**218,260**	**-2,409**
R7-R10	105531	102,647	2,884	158,916	149135	9,781
Total	294276	293,525	751	374,767	367,395	7,372

Last year the IEEE contacted all members by e-mail who had not renewed and in only a single day over 2400 members who were contacted processed their membership renewal. This tells me that a significant number of the 812 who didn't renew locally may just have put their renewal on a "to do" list and never got the process completed. I'm asking everyone to gently ask your co-workers, colleagues and students if they had renewed and if not, its still not too late for them!

Here's another benefit that new members may be able to take advantage of; if members begin their memberships in April, they will receive 9 months of membership for 50% of the normal annual dues. If anyone you know has been thinking about membership in the IEEE, this is the perfect time for them to join.

There may be a few members who are retiring or have just retired and might think it's not a good idea to renew their memberships. After all, you probably don't need the cutting edge information available from The IEEE on a regular basis. However, you might want to check and see when you will qualify for Life membership. Basically, you need 100 years total comprised of years of membership plus your age (65 yrs. old and 35 years of membership is typical). I'd hate to see someone drop out if they were only a year or two short of that requirement. For details, you can refer to the web page: http://www.ieee.org/portal/pages/committee/lmc/index.xml

Benefits for Life Members include:

- Dues and regional assessments are waived for a Life member
- For qualifying Life members, Society fees are waived (see the specific Society for details)
- Life members may receive reduced member rates at IEEE sponsored conferences. [Reduced fees, waiver of fees, or fee differential (are permitted at the discretion of the Conference Committee).
- Life Members continue to receive the same benefits that are available to other IEEE members
- IEEE Financial Advantage Program (includes IEEE Insurance Program)

IEEE Mentoring Connection

IEEE is offering its members the opportunity to participate in an online program which will facilitate the matching of IEEE members for the purpose of establishing a mentoring partnership. By volunteering as a mentor, individuals use their career and life experiences to help other IEEE members in their professional development. I believe this program can be a great tool to provide our newest members of our profession guidance in their careers and provide experienced members a chance to hear first hand from the newly graduated about the latest training the next generation is receiving. This is a program for higher level members and is provided to help ease the transition out of school and into a career.

As a mentee, you lead your partnership by selecting your mentoring partner from among those who have volunteered to serve in this capacity. I ask that you review the time and effort commitment to the program to ensure a successful mentoring partnership. Participation in the program is voluntary and open to all IEEE members above the grade of Student Member.

If you are interested, please go to http://www.ieee.org/mentoring for information on the roles and responsibilities of each mentoring partner. I encourage you to take advantage of the IEEE network of technical professionals or offer your expertise and sign up for the online mentoring program today.

Who can be an IEEE Mentor?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Able to communicate effectively with others
- Willing to share some career successes and failures
- Individuals who may be or have been executives, consultants, or in middle or upper management, or in research
- Individuals who may be or have been educators, entrepreneurs, or self-employed
- Individuals who may be or have been proven leaders offering inspiration and insight
- Individuals who may be or have been IEEE officers or volunteers
- Willing to review an orientation session to learn guidelines, tools of program and the mentee and mentor's role and responsibilities

Who can be an IEEE Mentee?

IEEE higher-grade members (above Student Member grade) who are, but not limited to:

- New professionals in their first or second job, or considering entering graduate programs
- Recent graduates entering the professional workforce for the first time
- Professional making a career move or career change
- Passionate for learning
- Willing to give time and effort to the mentoring partnership (we suggest minimum of two hours per month)
- Willing to identify and clarify their developmental goals
- Interested in learning from another professional "who has been there"
- Willing to participate in mentee orientation session to learn guidelines, and tools of program and their role and responsibilities as a mentee

This program deserves your consideration and doesn't require a large amount of time on your part. It can provide of great assistance to the next generation of engineers.

Russ Kinner
Membership Chair, Phoenix Section

RE-SEED

Retirees Enhancing Science Education through Experiments & Demonstrations

Overview

RE-SEED (Retirees Enhancing Science Education through Experiments and Demonstrations) is a Northeastern University program that prepares engineers, scientists, and other individuals with science backgrounds to work as volunteers, providing in-classroom support to upper elementary and middle school science teachers with teaching the physical sciences.

After completing a comprehensive free training program, participants volunteer in middle school classrooms on the average once a week for at least one year. RE-SEED began in 1991 with six volunteers. To date close to 500 RE-SEED volunteers have worked in schools in about 100 communities throughout the country offering about 500,000 hours of their time.

Nationally, 75 percent of 7th and 8th grade students are taught physical science by teachers who do not have a major or a minor in the subject (The National Science Board, Science and Engineering Indicators 2000). RE-SEED volunteers possess talent and expertise that complement those of science teachers. They bring with them a wealth of knowledge and experience that allows them to make science interesting and relevant to everyday situations.

RE-SEED volunteers work closely with the host science teachers to help them enrich and implement their school curriculum. Overall the volunteers become involved members of their schools' and even their districts' teaching team, sometimes taking part in curriculum adoption decisions.

Please contact us by email at reseed@neu.edu or phone 888-742-2424; Shelia Kirsch at Sheila.Kirsch@asu.edu and / or Deirdre Weedon, d.weedon@neu.edu. if you are interested in learning more about these training programs.

IEEE Computer Society - Phoenix Chapter

www.ewh.ieee.org/r6/phoenix/compsociety

NEXT MEETING

Speaker: Audrey Skidmore
Date: 6:00 P.M., Wednesday, April 4, 2007
Location: DeVry University, 2149 West Dunlap Ave, Phoenix, AZ 85021 (1 mile east of I-17 on Dunlap, SE corner of 22nd Ave and Dunlap). Networking will be in the Courtyard (6-7PM with light meal), presentation at 7PM.

Free, everyone is welcome. Please tell others about this meeting.

Introduction to GIS

Audrey, Computer Society Webmaster and Secretary, will discuss the Geographic Information Systems.

For more information about this meeting, contact c.vasquez-carrera@computer.org

May Meeting
Announcement for the
Phoenix Chapter of the
IEEE EMC Society

Date: Wednesday, May 2nd, 2007
Place: Garcia's Mexican Restaurant at Embassy Suites Hotel
Address: 4400 South Rural Road, Tempe, Arizona
Address: Just South of U.S. 60 on West side of Rural Rd.
Time: 5:30PM Social, 6PM Dinner (order off menu), 7PM Meeting and Presentation
Title: Understanding the Latest Changes to IEC 17025 for EMC Lab Accreditation
Speaker: Daniel D. Hoolihan, President of Hoolihan EMC Consulting

Abstract: ISO/IEC 17025 is used as the basis of accreditation for testing and calibration laboratories. This standard was recently updated in 2005. A summary and review of the 17025 standard will be conducted. This talk will include an analysis of the 2005 changes to the standard including a comparison of the technical and the administrative requirements.

About the speaker: Dan Hoolihan has been actively involved with the ANSI-Accredited Standards Committee on EMC since 1985. He has been an active member of the Steering Committee of C63, including acting as its recording secretary, for over 15 years. Hoolihan has been chairman of Subcommittee 6 (SC-6 - Lab Accreditation) and SC-8 (EMC and Medical Devices) since their inception. Dan is the past-president of the IEEE EMC Society (1998-1999) and has been on the Board of Directors of the EMC Society of the IEEE since 1987. He has held many positions with the EMCS board in his years of service. He most recently served as the Chair of the 2002 IEEE International Symposium on EMC which was held in Minneapolis in August of 2002. He helped found the EMC chapter of the Twin Cities Section in 1985 and has been active in the local chapter since that time. Hoolihan has been consulting in EMC Engineering since January of 2000. He specializes in EMC-Laboratory evaluations, EMC standards, and EMC Education. He is a consultant to the United States Department of Commerce National Institute of Standards and Technology (NIST) in the area of Telecom Certification Body (TCB) and Conformity Assessment Body (CAB) evaluations. He is also an EMC and Telecom assessor for the NIST National Voluntary Laboratory Accreditation Program (NVLAP).

RESERVATIONS: Please call Daryl or Mary at Kimmel Gerke Associates in Mesa AZ at 480-755-0080. (If no answer, please leave a voice mail.) You may also register by email at dgerke@emiguru.com. There is no charge for meetings, but you pay for your own meal and drinks. Since we order off the menu, we do not need an exact number, so if you decide at the last minute, please come anyway. You don't need to be an IEEE or EMC Society member to attend -- all are welcome.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS
WAVES AND DEVICES
PHOENIX CHAPTER

April 6, 2007 Meeting
Sponsored by AINE/CSSER
www.eas.asu.edu/~wadweb

Recent Advances in Silicon and Non-Silicon Nanotechnologies for High-Speed and Energy-Efficient VLSI Nanoelectronic Applications

Dr. Robert Chau
Intel Senior Fellow
Director of Transistor Research and Nanotechnology
Intel Corporation

Abstract

This presentation will summarize some of the most recent progress made in Si nanotechnologies for advanced CMOS transistors in the nanotechnology era. Through these Si innovations, it is expected that CMOS scaling and performance trends will extend and continue well into the next decade. Furthermore, there has been much interest generated and good progress made in the research of non-silicon electronic materials and nanoelectronic devices, and their integration onto silicon for future high-speed and energy-efficient VLSI nanoelectronic applications. The challenges and opportunities of these emerging non-Si nanotechnologies and nanoeelctronic devices, and their integration onto the existing silicon platform, will be discussed in this presentation.

Biography

Dr. Robert Chau is an Intel Senior Fellow and the Director of Transistor Research and Nanotechnology at Intel Corporation. He is responsible for directing research and development in advanced transistors and gate dielectrics, process modules and technologies, and integrated processes for microprocessor applications. He is also leading research efforts in novel electronic materials and emerging non-silicon nanotechnologies for future nanoelectronics applications. Dr. Chau holds more than 120 issued United States patents, has received six Intel Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards for his technical achievements, was recognized by *IndustryWeek* in 2003 as one of the 16 "R&D Stars" in the United States who "continue to push the boundaries of technical and scientific achievement," was the recipient of the 2003 Alumni Professional Achievement Award from The Ohio State University, is currently a member of the Board of Directors of the Oregon Nanoscience and Microtechnologies Institute (ONAMI) and a member of the Scientific Advisory Board of the Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN) in Ireland, and is a Fellow of the IEEE.

Date: April 6, 2007
Location: Arizona State University, Main Campus, Goldwater Center (GWC) Room 487
See http://www.asu.edu/map/b2.html for more details.
Time: 4:00-5:00pm Presentation,
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS
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April 11, 2007 MTTS Meeting
www.eas.asu.edu/~wadweb

Measuring AC Response of a Carbon Nanotube Field-effect Transistor

Dr. Islamshah Amlani

Embedded Systems Research, Motorola Labs, Motorola, Inc.

Abstract

Nanoelectronic devices based on carbon nanotubes, nanowires, and other variations are emerging with interesting and novel properties. Specifically, single-walled carbon nanotube based field-effect transistors (FETs) are considered promising candidates for high frequency applications with a predicted frequency response in the terahertz regime. The main reason for this anticipation is the ballistic transport in the channel over several hundred nanometers at room temperature leading to high transconductance and mobility values. Despite tremendous interest in the AC properties of nanotube FETs, a full RF characterization of SWNT-FETs has proven challenging to date. As a result, indirect measurement approaches have been employed to assess the frequency response of these devices.

In this presentation, the speaker will briefly summarize some of the recently demonstrated attempts to assess frequency response of nanotube FETs. The bulk of the presentation will comprise of a recently developed technique to measure AC voltage gain from a nanotube FET. Both experimental and theoretical results will be discussed.

Biography

Islamshah Amlani received the M.S. and Ph.D. degrees in Electrical Engineering from the University of Notre Dame in 1997 and 1999, respectively. He worked as a postdoctoral researcher at the University of Notre Dame for a brief period before joining Motorola in the beginning of 2000. Currently, Islamshah holds a position of principal staff scientist at Embedded Systems Research, a part of Motorola Labs - the corporate R&D laboratories of Motorola, Inc. He has been actively involved in the research of nanoelectronics and quantum devices for more than a decade, and has published close to 50 technical papers in this field including a book chapter. He also holds 2 US patents with 8 more pending. He was the Grand Prize Winner of the prestigious Worldwide Merrill Lynch Innovations Grant competition in 1999 and the recipient of Global Indus Technovator Award at MIT in 2003. The focus of his current research interest includes flexible electronics and RF and microwave applications of nano-enabled devices using technologies such as carbon nanotubes and nanowires. He is a member of IEEE.

Date: Wednesday, April 11, 2007
Location: Arizona State University, Main Campus, Goldwater Center (GWC) Room 487
See http://www.asu.edu/map/b2.html for more details.
Time: 6:00-7:00pm Presentation, 7:00pm Dinner (Pizza & soda are being provided by the WAD Phoenix Chapter)
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS
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April 26, 2007 MTTS Meeting
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High Mobility III-V MOSFET Technology

Dr. Matthias Passlack

Wireless Packaging Systems Laboratory
Freescale Semiconductor, Tempe Az

Abstract

Novel device architectures, high-κ gate dielectrics, metal gates and high mobility channel materials will be required to continue CMOS device scaling according to Moore's Law and the ITRS. In the shorter term, high mobility III-V MOSFET development will likely be more driven by RF applications. In recent years, fundamental oxide/semiconductor interface issues have been overcome and high mobility III-V MOS technology has advanced to the level of device fabrication. In Freescale, we have demonstrated channel electron mobilities exceeding 12,000 and 6,000 cm^2/Vs in high-κ dielectric (κ ≈ 20) InP and GaAs based MOSFET structures, respectively. In collaboration with the University of Glasgow, we have manufactured 1 μm n-channel GaAs enhancement-mode MOSFETs designed for RF power applications based on a novel device architecture. The 1 μm n-channel, metal-gate GaAs MOSFETs operate in enhancement mode with the following DC figures of merit: threshold voltage = 0.27 V, transconductance = 457 mS/mm, saturation current= 398 mA/mm and subthreshold swing = 98 mV/dec with gate current < 60 pA. In this seminar, I will review oxide/semiconductor interface properties and characterization, wafer fabrication, high mobility transistor design, channel mobility, transistor data, and predicted small III-V MOSFET performance.

Biography

Matthias Passlack received the Dipl.-Ing. (M.S.) and Dr.-Ing. (Ph.D.) degrees, both in Electrical Engineering, from the University of Dresden, Germany, in 1984 and 1988, respectively. In 1993, he joined AT&T Bell Laboratories in Murray Hill, NJ, where he pioneered a ground breaking approach towards low defect density oxide/GaAs interfaces, a problem which had eluded scientists for more than 30 years. In 1995, he joined Motorola's Corporate Research Laboratories in Tempe, AZ. Over the last 12 years, he has led various R&D efforts at Motorola and Freescale Semiconductor in the field of III-V MOS materials, processes, characterization, devices, and physics. He is a Distinguished Member of the Technical Staff at Freescale Semiconductor.

Dr. Passlack has published two book chapters and over 60 technical articles in peer reviewed international journals, and holds 18 US patents. His work was featured in "GaAsing Up Cellphones" IEEE Spectrum, pp. 15-16, May 2006.

Date: Wednesday, April 26, 2007
Location: Arizona State University, Main Campus, Goldwater Center (GWC) Room 487
See http://www.asu.edu/map/b2.html for more details.
Time: 5:00-6:00pm Presentation, 6:00pm Dinner (Pizza & soda are being provided by the WAD Phoenix Chapter)
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.